HIRDLS

SW-HIR-2001

Originator: Charles Cavanaugh Date: 10 Dec. 2012

Subject/Title: **The Requirements of the HIRDLS Level 1 Correction Processor**

Description/Summary/Contents:

The purpose of this document is to capture the requirements of the High Resolution Dynamics Limb Sounder (HIRDLS) Level 1 Correction Processing System, and correctly and comprehensively catalog those requirements in an unambiguous form.

The goal of this document is to detail those requirements at a level that allows system architectural analysis to create a blueprint for construction.

Keywords:

Purpose of this Document:

Oxford University
Atmospheric, Oceanic &
Planetary Physics
Parks Road
OXFORD OXI 3PU
United Kingdom

University of Colorado, Boulder
for Limb Atmospheric Sounding
3450 Mitchell Lane, Bldg. FL-0
Boulder, CO 80301

Center

EOS

The Requirements of the HIRDLS Level 1 Correction Processor

Charles Cavanaugh

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1 Document Purpose and Goal

The purpose of this document is to capture the requirements of the High Resolution Dynamics Limb Sounder (HIRDLS) Level 1 Correction Processing System, and correctly and comprehensively catalog those requirements in an unambiguous form. The goal of this document is to detail those requirements at a level that allows system architectural analysis to create a blueprint for construction.

2 Functionality of the System

The HIRDLS Level 1 (L1) Correction Processing System, hereby known as the L1C Processor, is to ingest a HIRDLS L1 Hierarchical Data Format (HDF) file (known as a HIRDLS1 file), correct for the radiometric effects of the accidental partial Kapton® blockage of the aperture, and create a HIRDLS1C file that contains the geo-located, calibrated and corrected data, as well as other ancillary data needed in subsequent processors. Those subsequent processors, when combined with the L1C Processor and any preceding processor(s), form a Product Generation Executive (PGE) that creates the required HIRDLS standard data products. The L1C Processor creates a standard data product known as the HIRDLS1C file, which has the exact same structure as the HIRDLS1 file. The content and structure of the HIRDLS1 file has been enumerated in the HIRDLS L1 Processor Requirements document, and will not be duplicated here. A detailed description of the Kapton® blockage can be found in Gille et al., [2008], High Resolution Dynamics Limb Sounder (HIRDLS): Experiment Overview, Results and Validation of Initial Temperature Data, *Journal of Geophysical Research*, VOL. 113, D16S43, doi:10.1029/2007JD008824.

3 External Interfaces

The L1C Processor is to interact with the EOSDIS Core System (ECS) Project Science Data Production (SDP) Toolkit to perform certain required tasks, including time conversion, process control file interaction, and metadata writing. The SDP Toolkit is a suite of functions, written in the C language, with C language primitives and Toolkit-specific data types as arguments in their contracts. The Toolkit is provided as a dynamic-link UNIX-specific library. For further information on the Toolkit, please see the ECS document 333-CD-004-001, Release B.0 SCF Toolkit Users Guide for the ECS Project.

The L1C Processor is also to interact with the HIRDLS Science Investigator-Led Processing System (SIPS). The SIPS creates the environment for the L1C Processor to run, invokes the L1C Processor, and also post-processes the L1C Processor output. The SIPS was created to be a mini-EDOS (EOS Data and Operations System), and because of that, certain conventions must be followed, including using a Process Control File (PCF) to envelope all processor systems run in SIPS, including the L1C Processor. Other interactions with SIPS are negotiable with the SIPS team, including ancillary data ingestion by processors, post-processing status handling, and hardware requirements.

4 Constraints

Certain constraints (HDF file generation, interacting with a C-written library) have already been introduced, but beyond those, the only constraint is hardware-oriented, which are ever-changing, as CPUs get faster (and more plentiful) and memory gets cheaper, and therefore those constraints are to be negotiated with the SIPS team and the HIRDLS Project Manager.

5 Interaction

There need be no graphical interface to the L1C Processor, nor does there need to be interaction during the execution of the L1C Processor. The system is considered to be a stand-alone scientific application, capable of running in the environment and on the platform chosen via negotiation with the HIRDLS Program Manager.

6 Overview

Given the information in the preceding sections, a visual overview of the system is as follows in Figure 1. SIPS and SDP Toolkit have been introduced in Section 3, and any further discussion of these is beyond the scope of this document. The input HIRDLS1 file and the output HIRDLS1C file, while introduced in Section 2, will be discussed in further sections.

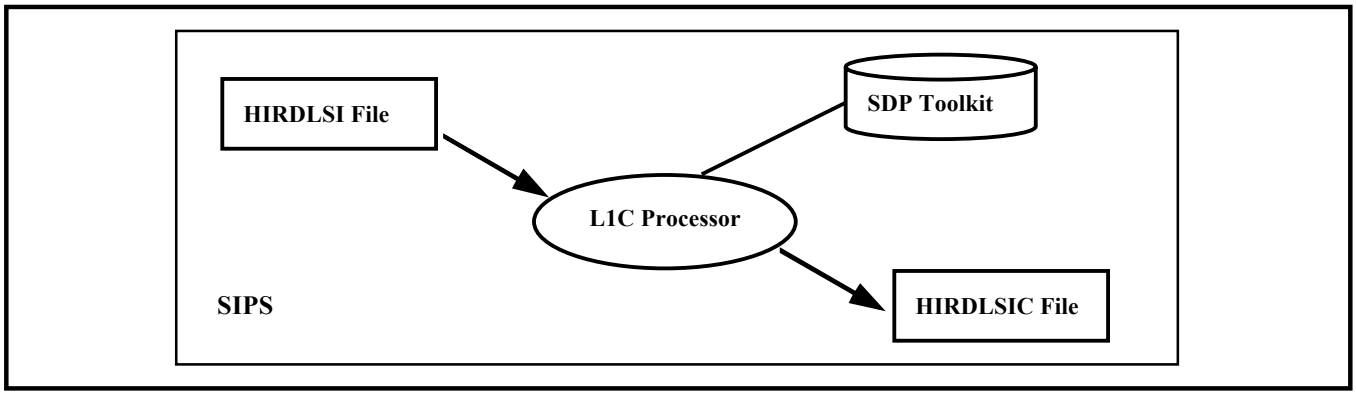

Figure 1 L1C Processor Overview

7 Input

As first noted in Section 2, the L1C Processor takes one HIRDLS1 file as input. The exact structure and contents of the HIRDLS1 file is detailed in the HIRDLS L1 Processor Requirements document.

Also input to the L1C Processor is various files that contain information to: 1) characterize the Kapton® blockage; 2) characterize the radiometric noise; and 3) describe the metadata content necessary for delivery to EDOS. These files are considered part of the L1C Processor, and are to be included in its deliveries. The format and content of these files is negotiable with the HIRDLS science team (in the case of 1 and 2), and with the HIRDLS Program Manager and EDOS Liaison (in the case of 3). As the L1C Processor progresses through development, this list of system input files could grow or shrink.

8 Output

As first noted in Section 2, the L1C Processor generates one HIRDLS1C file as output. The content and structure of the HIRDLS1C file is the exact same as the HIRDLS1 file, with only the radiometric content, but not structure, varying. All non-radiometric fields must contain the exact same content and structure as in the input HIRDLS1 file. Because the output HIRDLS1C file has the same structure as the input HIRDLS1 file, the details of the output HIRDLS1C file will not be enumerated here. As noted in Section 7, these details can be found in the HIRDLS L1 Processor Requirements document.

9 Algorithms

The algorithms found in the L1C Processor are restricted to those necessary to correct for the partial Kapton® blockage. Any enumeration of these algorithms is beyond the scope of this document, but will be introduced in the HIRDLS L1C Processor Architecture document.