# HIRDLS


## HIGH RESOLUTION DYNAMICS LIMB SOUNDER

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# SP-HIR-279
# IPS to PSS Interface Control Document (ICD)

Approved by:

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/s/ Nigel Morris, HIRDLS UK Program Manager Date

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/s/ Dexter Duncan, SPU Responsible Engineer Date

# Log of Changes

| Rev | Date | Section | Change Description | |
|---|---|---|---|---|
| | 98-08-18 | | Initial Release | |
| A | 00-06-02 | Sig. Page | Updated to reflect current program responsibility | |
| | | 2.1 | Changed ITS entry from SP-HIR-013 to GSFC 424-28-21-13<br>Provided release dates for Applicable documents | |
| | | 3.2.1.2 | Deleted spurious reference to SP-HIR-169; substituted pointer to Section 3.2.3. | |
| | | 3.2.2.1.1(a) | Added definition of 28V QA and QB | |
| | | 3.2.2.1.1(b) | Added definition of 28V QA and QB<br>Changed PCU 28V Reg power to 30 Vdc | |
| | | 3.2.2.1.2 | Paragraph b: Updated +28 V regulated voltage tolerance from 27.5-28.5 to 29.5-30.5.<br>Table 3.2.2.1.2-1 converted all data to table format. Added cable resistance and voltage drop.<br>Corrected headers to reflect 28V QA, 28V QB and 28V Reg. | |
| | | 3.2.2.3 | Fig. 3.2.2.3-1: updated star-point and return line scheme per current design; A- and B-side 28 Reg. return lines combined. Removed dashed line for “Link” to reflect current design. Correct Signal names for A & B IPU_28REG_RTN. | |
| | | 3.2.2.4.1 | Updated ±15 V voltage limits per CR-118.<br>Created Table 3.2.2.4.1-1. Converted data to table format. Added information from Table 3.2.2.4.2-1. | |
| | | 3.2.2.4.2 | Removed “Power” from title.<br>Removed “cross-strapping” from assumptions<br>Deleted Table 3.2.2.4.2-1. | |
| | | 3.2.5.2 | Table 3.2.5.2-2. Added comment that Opto-coupler signal, return and shield for Opto-5 & 6 are not connected in PCU. | |
| | | 3.2.2.6 | Fig. 3.2.2.6-1: separated 5 V and 15 V A- and B-side return lines; renamed “SSP” on PCU side to “Chassis Ground Terminal”, per current terminology. Removed dashed line for “Link” to reflect current design. Removed TBDs. | |
| | | 3.2.3 | Figure 3.2.3-1: Changed PCU-side ground terminal designation to “Chassis Ground Terminal”. Converted “TBD”s to “IPU_COM_GND”. Deleted unused opto-coupler inputs from IPU. | |
| | | 3.3 | Deleted obsolete reference to TC-UCB-009. | |
| B | 00-10-17 | 3.2.2.3 | Figure 3.2.2.3-1. Changed from twisted eights to twisted pairs to match as-built cable. Corrected mnemonics of 28REG returns to reflect SP-HIR-169G. Showed that link to IPU common ground is not installed in the IPU. | |
| | | 3.2.3 | Figure 3.2.3-1. Removed first two IPU common ground wires from cable. | |
| | | 3.2.5.2 | Table 3.2.5.2-1. Corrected group designations to match the as-built cable and Figure 3.2.2.3-1. Removed Side A/B from signal names on 28Reg. return lines. | |

| Rev | Date | Section | Change Description | |
|---|---|---|---|---|
| | | | Table 3.2.5.2-2. Changed pins 30 and 69 on J914P to "blank". Added signal names for pins 22,29,38, and 39. | |
| | 00-12-05 | 3.3 | Modified entire section to accommodate C&TH requirements. (CR189) | |
| | | 4.0 | Added C&TH acronyms to list. (CR189) | |
| | 01-01-11 | 3.3.1.2 | Table 3.3.1.2. Replaced TBDs with scaling factors provided by J. Whitney | |
| | 01-02-22 | Sig. page | Added Jerry Drake to approve changes to command and telemetry IF. | |
| | | 3.2.3.1 | Removed words "active low" from clock definition per RE's comments | |
| | | 3.3.1.1 | Changed per RE's comments:<br>PSS_STATUS_06<br>changed bit 6 definition to "Logic 0"<br>changed bit 8 definition to "GND"<br><br>PSS_STATUS_07<br>changed bit 7 definition to "Logic 0"<br>changed bit 8 definition to "GND" | |
| | 01-02-28 | 2.1 | Removed SP-HIR-200G from list of referenced documents | |
| | | 3.2.2.1.1 | Removed reference to SP-HIR-200G and replaced with reference to<br>Table 3.2.2.1.2-1. | |
| C | 01-04-16 | 3.2.2.1.5 | Figure 3.2.2.1.5-1. Added number of PCU ground terminal to depiction of Cable U7. (CR190) | |
| | | 3.2.3 | Figure 3.2.3-1. Added number of PCU ground terminal to depiction of Cable U8. (CR190) | |
| | 01-04-17 | 3.2.2.1.2 | Table 3.2.2.1.2-1. Added line for minimum voltage rise times. (CR205) | |
| | | 3.2.2.1.3 | Added section to define inrush current. Added Figures 3.2.2.1.3-1 through 3.2.2.1.3–5. (CR205) | |
| | | 3.2.2.1.4 | Renumbered section. (CR205) | |
| | | 3.2.2.1.5 | Renumbered section, including figure. (CR205) | |
| | | 3.2.2.2 | Renumbered section. (CR205) | |
| | | 3.2.2.2.1 | Renumbered section. (CR205)<br>Modified Table 3.2.2.2.1-1.<br>Added "TBR" to voltage limits at PCU end of cable. (CR205)<br>Added line for minimum voltage rise times. (CR205) | |
| | | 3.2.2.2.2 | Renumbered section including Table. (CR205) | |
| | | 3.2.2.2.3 | Added section to define inrush current. Added Figures 3.2.2.2.3-1 through 3.2.2.2.3–4. (CR205) | |
| | | 3.2.2.2.4 | Renumbered section. (CR205) | |
| | | 3.2.2.2.5 | Renumbered section, including figure. (CR205) | |
| | 01-06-11 | 3.2.5.2 | Table 3.2.5.2-1 Correct spelling error (RE comments to CR205) | |
| | | 3.3.1.1 | Table 3.3.1.1-1 Corrected Table number<br>Corrected table entries per RE inputs (CR205) | |
| | | 3.3.1.2 | Table 3.3.1.2-1 Corrected table entries per RE inputs (CR205) | |

| Rev | Date | Section | Change Description | |
|---|---|---|---|---|
| D | 01-05-01 | 3.3.3 | Added section 3.3.3, Discrete Pulses from IPU to PSS from C&TH Vol. I, paragraph 2.9.4.2 (CR200) | /s/ J.Whitney |
| | | 3.3.4 | Added section 3.3.4, Individual Relay Control (IRC) Words from C&TH Vol. I, paragraph 2.9.4.3 (CR200) | R.von Savoye |
| | | 3.3.5 | Added section 3.3.5, PSS Function Codes & PSM Code Sequences from C&TH Vol. I, paragraph 2.9.4.4 (CR200) | N.Morris |
| | 01-07-27 | 3.2.2.1 | Figure 3.2.2.1.5-1 (U7). Added 1kΩ connections from +28 V Reg. A & B Loads to IPU 28 Reg. Return Star Point Terminal. ( DR AB9576, CR215) | R.Lindgren |
| | | 3.2.3 | Figure 3.2.3-1 (U8). Added 1KΩ resistors and 1 μF capacitors on IPU side to reflect rework authorized by DR AC1862. Add links between twisted pairs to ensure proper grounding. (CR215) | D.Duncan<br>J.Drake |
| | | 3.3.1.1 | Table 3.3.1.1-1, Data Word 4003, bit 2: changed from "+28N" to "+28NC", Data Word 4006, Data bit 3 and 5: changed "+28Q" to +28QC" (CR200) | |
| | | | | |

## TABLE OF CONTENTS

# 1 SCOPE

Interface Control Documents (ICDs) in the SP-HIR-2XX series define, as applicable, the specific design implementations of the electrical, functional, mechanical, conductive thermal, and optical interfaces between specified HIRDLS Subsystems or, in a few special cases, between units within the same subsystem.

This ICD defines the specific design implementation of the interfaces between the Instrument Processor Subsystem (IPS) and the Power Supply Subsystem (PSS). The interfaces between these two subsystems are limited to the Electrical interfaces between the Power Converter Unit (PCU) and Instrument Processor Unit (IPU), and between the PCU and Signal Processing Unit (SPU).

# 2 DOCUMENT REFERENCES

## 2.1 Applicable Documents

The documents listed below are a part of this ICD to the extent specified herein. In the case of a conflict between the contents of this ICD and any Applicable Document, this ICD shall take precedence.

| | | |
|---|---|---|
| SP-HIR-169G | HIRDLS Power Distribution, Switching and Grounding | 00-02-01 |
| ANSI/TIA/EIA 422-B-1994 | Electrical Characteristics of Balanced Voltage Digital Interface Circuits | |
| GSFC 422-11-12-1 Rev B | General Interface Requirements Document (GIRD) | August 1998 |
| GSFC 424-28-21-06 | Unique Instrument Interface Document for HIRDLS (UIID) | April 1998 |
| GSFC 424-28-21-13 | Instrument Technical Specification (ITS) | February 2000 |

## 2.2 Information Documents

The documents listed below are for information only and are explicitly not, by reference, part of this ICD.

| | | |
|---|---|---|
| SP-HIR-103 | Command and Telemetry Handbook | Current Revision |
| SP-HIR-217 | STH to IPS Interface Control Document | Current Revision |

# 3 INTERFACE REQUIREMENTS

## 3.1 Interface Concept Overview

The electrical interfaces between the IPS and the PSS consist of power, grounding, control signals, and data signals. There are no mechanical, thermal, or optical interfaces between them. The Power Converter Unit (PCU) will provide unswitched primary and switched secondary power to the Instrument Processor Unit (IPU), and switched secondary power to the Signal Processing Unit (SPU). The PCU will also provide power indirectly, through the IPU, to the Sun Sensors, Sunshield Door, IFC, and TSS heaters.

The PCU shall provide a fully redundant power interface with the IPU. When either the Spacecraft Quiet Bus A or Quiet Bus B is energized, the PCU shall pass this primary unswitched power to the respective side of the IPU. Once the processor within the IPU is initialized and communications with the spacecraft and ground have been established, the IPU can then command the PCU to switch on individual power to the SPU and other subsystems.

A top-level block diagram of the IPS-PSS interface is shown in Figure 3.1-1.

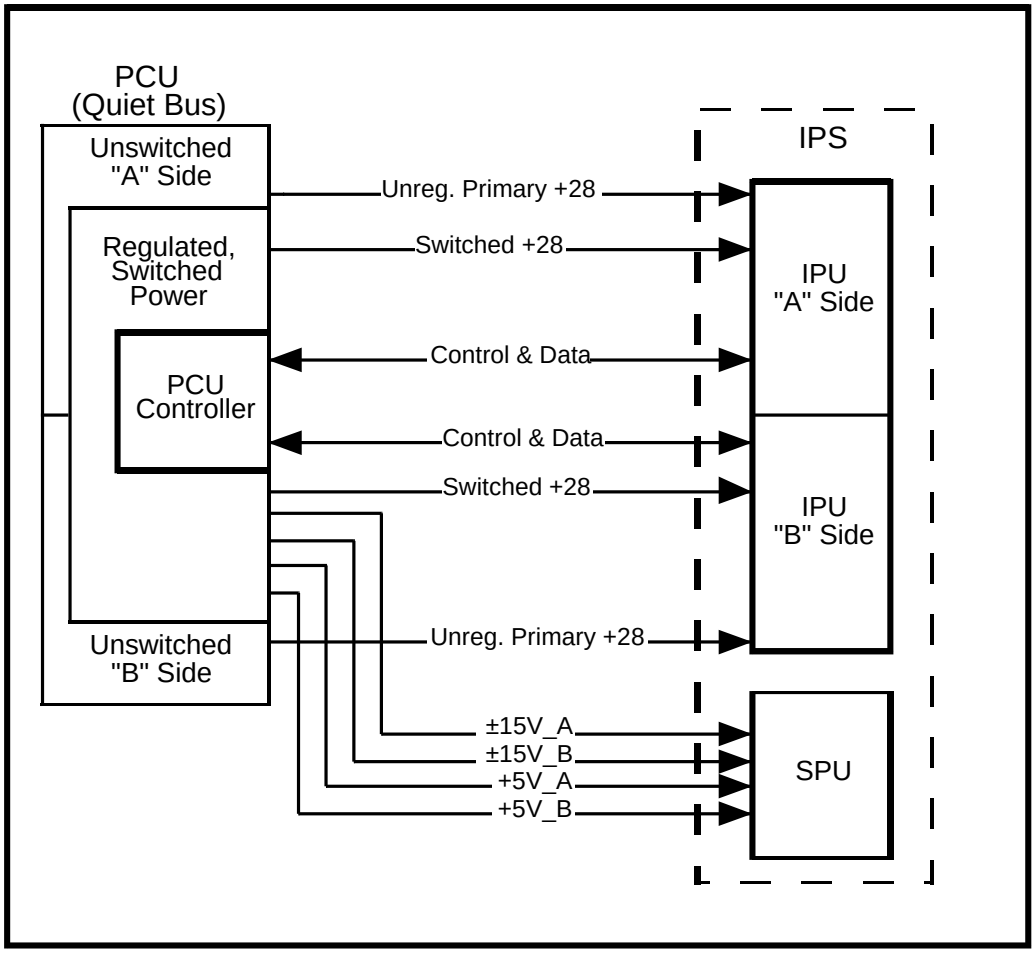


**Figure 3.1-1 IPS-PSS Interface Block Diagram**

## 3.2 Electrical Interface

Figure 3.2-1 shows the cables and connectors associated with the IPS-PCU interface.

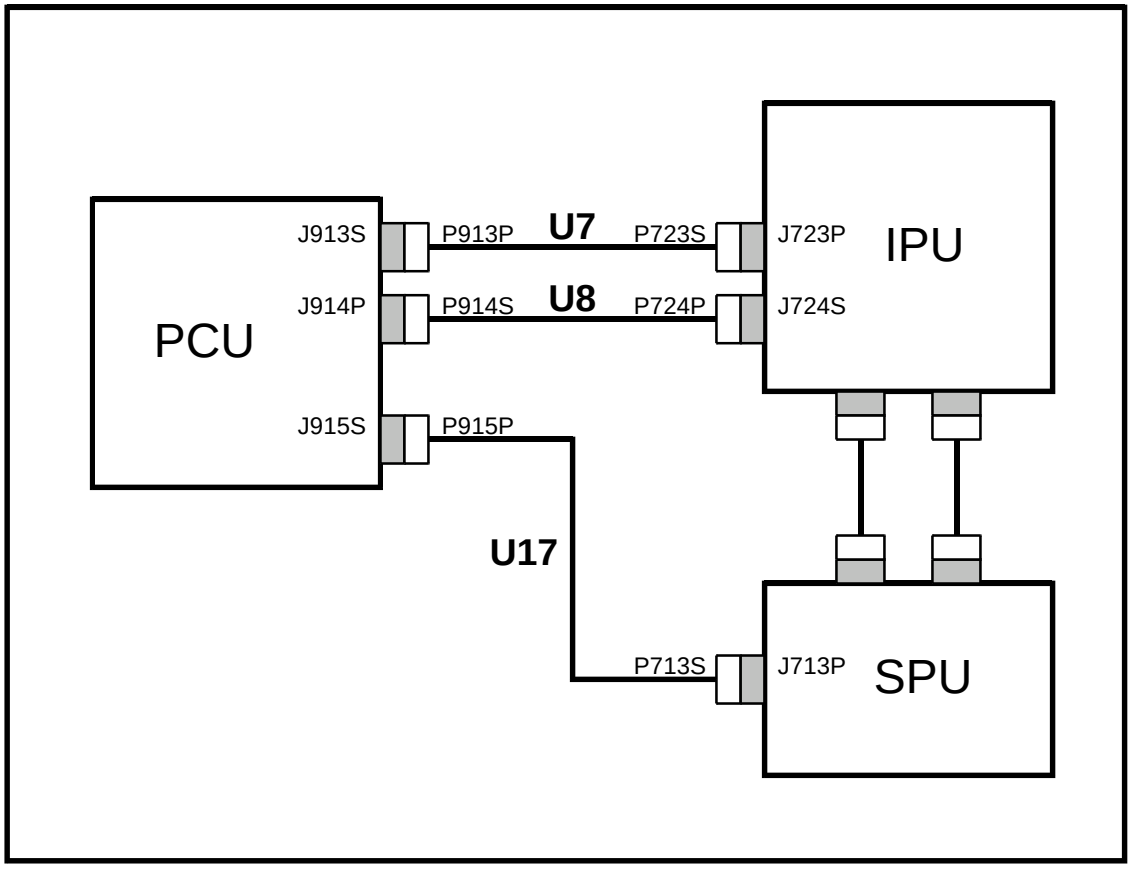


**Figure 3.2-1 IPS-PSS Cable/Connector Identification**

### 3.2.1 Grounding and Shielding

#### 3.2.1.1 Primary and Secondary Power Grounding and Isolation

The configuration of all grounds and returns within the PCU, the IPU, and the SPU, and their interconnections across the PSS-IPS interfaces, shall conform to the requirements of SP-HIR-169.

#### 3.2.1.2 Signal Grounds

See Section 3.2.3, Control and Data Interface.

#### 3.2.1.3 Equipment Enclosure Grounding, Shielding, and Bonding

Refer to SP-HIR-217 for equipment enclosure grounds.

#### 3.2.1.4 Wire and Cable Shield Grounds

Cables shall have an overall shield connected to chassis ground through the connector shells at both ends of the cable. Shields for groups of conductors within cables shall be insulated from other internal and overall shields, and shall be connected via connector pins as indicated in the relevant interconnection diagrams and pinout tables.

### 3.2.2 Power Interface

### 3.2.2.1 PCU-IPU Power Interface

#### 3.2.2.1.1 PCU Power Outputs to IPU

The PCU shall supply electrical power directly to the IPU via two fully redundant paths. The A-side of the PCU shall supply power to the A-side of the IPU and the B-side of the PCU shall supply power to the B-side of the IPU. The PCU shall furnish two types of power to the IPU:

a. Unregulated, non-switched +28 Vdc (nominal) primary power from the spacecraft Quiet Bus (referred to as "IPU_+28QA" and "IPU_+28QB"). [Note for Reference: Per the HIRDLS UIID, Section 5.1.1, the spacecraft primary power voltage shall be +29 ±2 Vdc under normal operating conditions; shall not deviate from the steady-state supplied voltage by more than ±2.9 V due to Instrument transients as specified in GIRD 5.2.5.2.3; under fault conditions shall not exceed +36 V continuously, or +42 V for transients of duration not exceeding 10 ms.]

b. Switched, regulated +30 Vdc from DC-DC converters within the PCU (referred to as "A_IPU_+28REG" and "B_IPU_+28REG."). Characteristics of this power at the PCU output connector shall conform to the requirements of Table 3.2.2.1.2-1 below.

The unregulated primary power, defined in paragraph a. above, shall be present at the IPU interface whenever the spacecraft bus is powered; i.e. when either spacecraft bus is powered the respective IPU side (A or B) shall receive unregulated primary power without command.

#### 3.2.2.1.2 IPU Power Inputs

At the inputs to the IPU, the power characteristics provided in Table 3.2.2.1.2-1 shall be met:

**Table 3.2.2.1.2-1 PCU to IPU Power Characteristics**

| | **IPU_+28QA and IPU_+28QB** | **A_IPU_+28REG and B_IPU_+28REG** |
|---|---|---|
| Voltage limits at PCU end of cable | +24.0<br>+35.0 | +29.5<br>+30.5 |
| Voltage limits at IPU end of cable | +23.8<br>+35.0 | 29.35<br>30.5 |
| IPU Nominal DC load current (mA) (1) | 1124 | 240 |
| IPU Peak DC load current (mA) (2) | 1309 | 1440 |
| Maximum resistance of cable + connector pins | 150 mΩ | 150 mΩ |
| PCU-induced ripple at PCU end of cable | <5% pp of nominal voltage, 1 Hz to 10 MHz | <0.25 Vpp, 1 Hz to 10 MHz |
| Inrush current: | Per GIRD section 5.2.5.2.1 | |

(1) 2-orbit average
(2) Over any 10 millisecond peak period

### 3.2.2.1.3 Inrush Current

The PCU shall perform to all requirements when connected to the IPU having the capability of sinking inrush currents as shown in Figures 3.2.2.1.3-1 through 3.2.2.1.3-5.

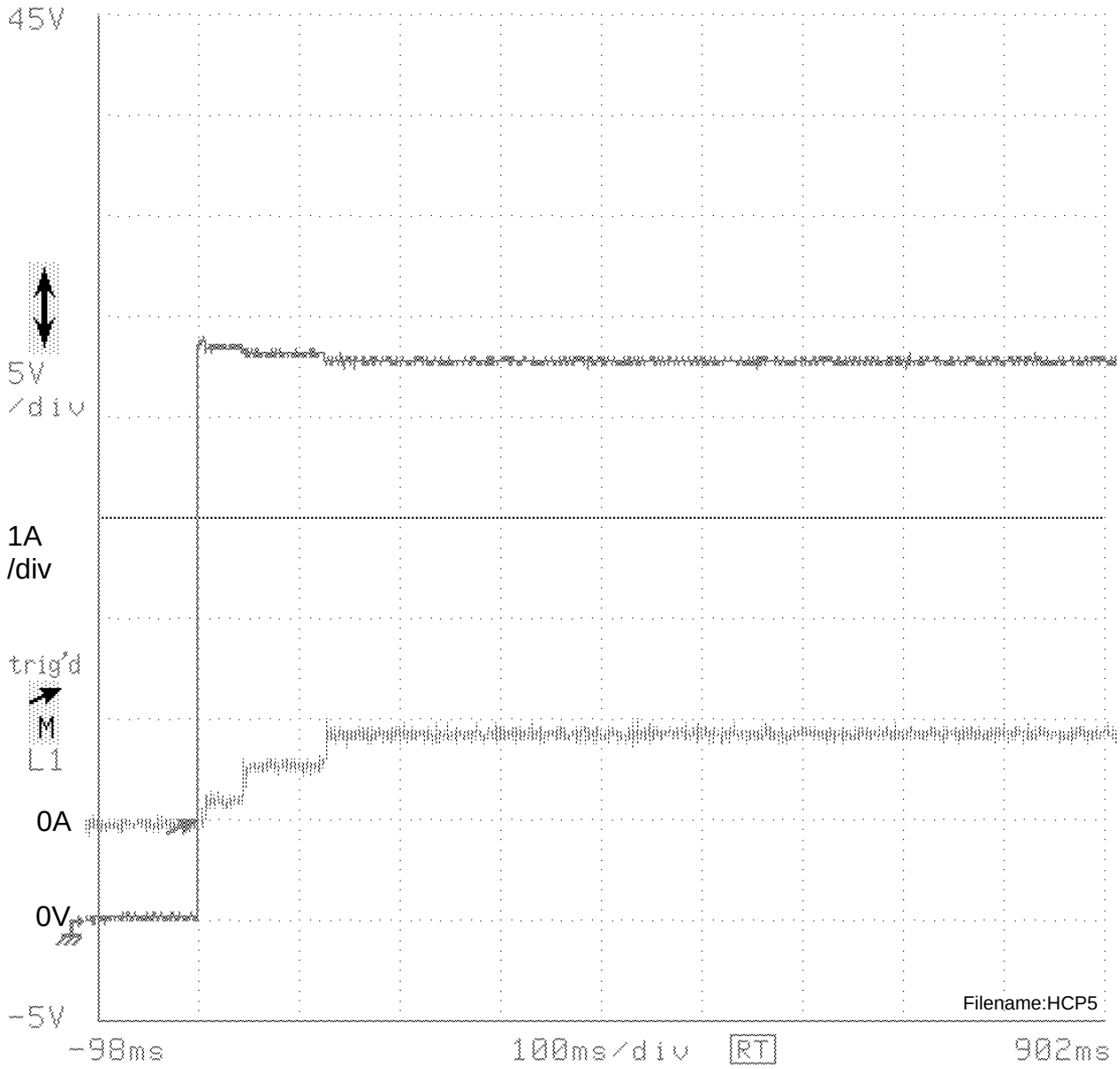


**Figure 3.2.2.1.3-1. IPU 28V Quiet Bus Inrush When Driven by an Ideal Power Supply.**

Vertical Scale: 1.0A/div., 5V/div.; Horizontal Scale: 100ms/div.

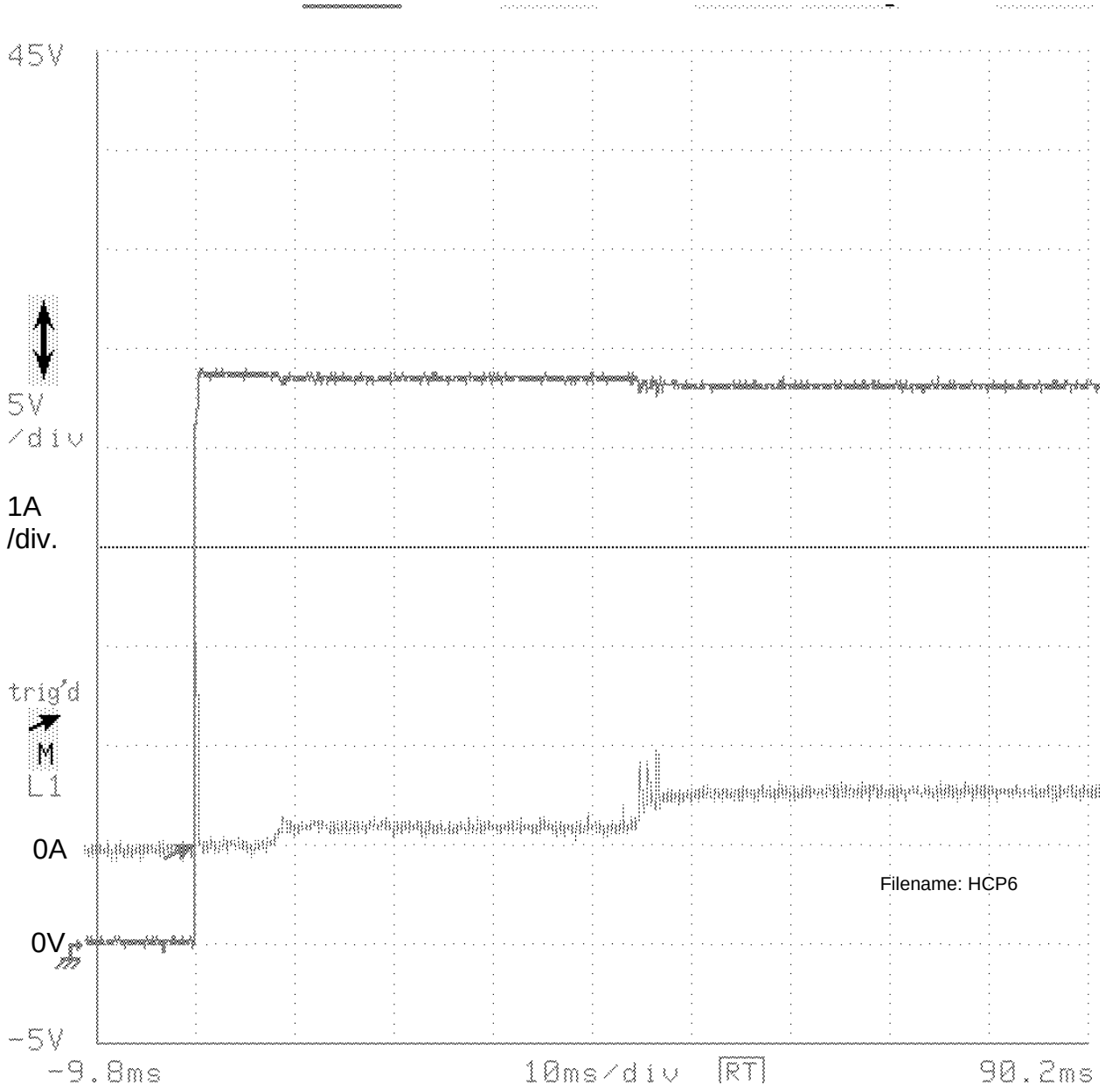


**Figure 3.2.2.1.3-2. IPU 28V Quiet Bus Inrush When Driven by an Ideal Power Supply.**

Vertical Scale: 1.0A/div., 5V/div.; Horizontal Scale: 10ms/div.; Peak Current: ~ 2.1A.

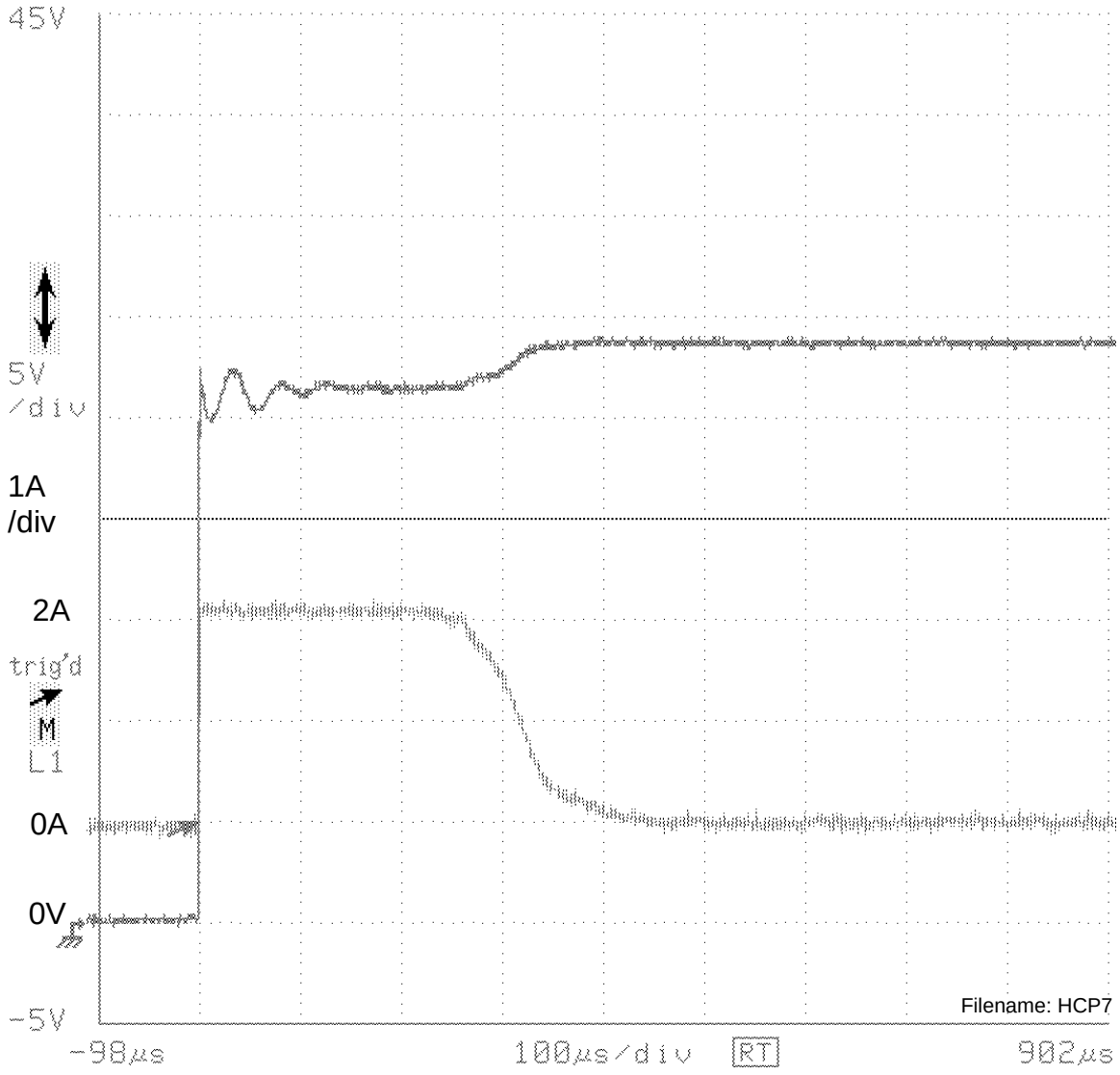


**Figure 3.2.2.1.3-3. IPU 28V Quiet Bus Inrush When Driven by an Ideal Power Supply.**

Vertical Scale: 1.0A/div., 5V/div.; Horizontal Scale: 100µs/div.; Peak Current: ~ 2.1A.

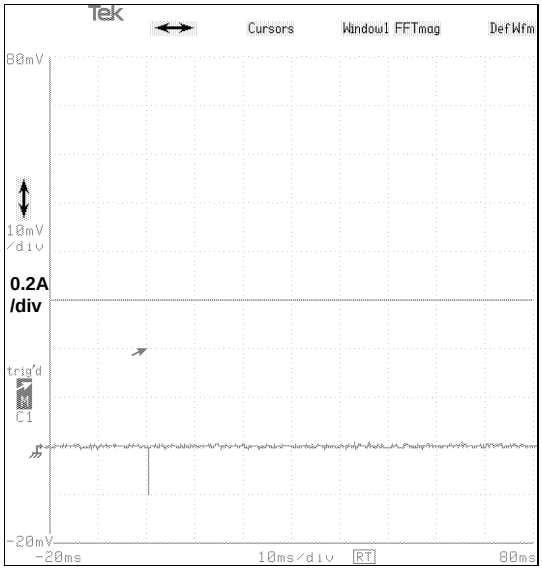


**Figure 3.2.2.1.3-4. IPU 28Reg Inrush When Driven by an Ideal Power Supply.**

Vertical Scale: 0.2A/div.; Horizontal Scale: 10ms/div.

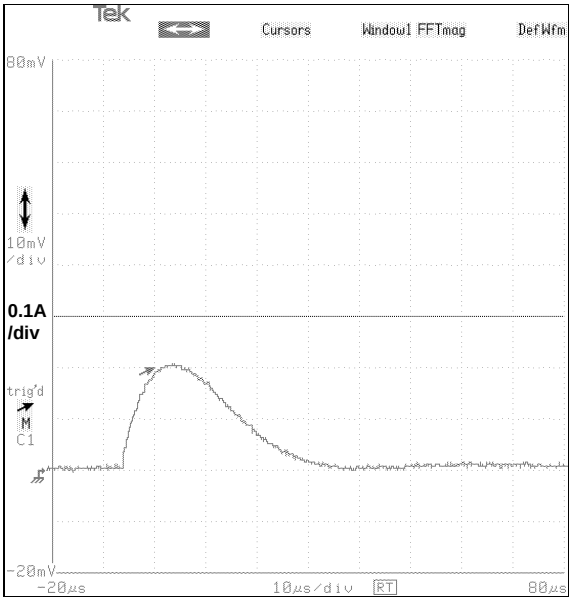


**Figure 3.2.2.1.3-5. IPU 28Reg Inrush When Driven by an Ideal Power Supply.**

Vertical Scale: 0.1A/div.; Horizontal Scale: 10µs/div.; Peak Current: ~0.2A.

#### 3.2.2.1.4 IPU Fault Tolerance

The IPU shall not be damaged by sustained voltages below the minimum indicated in Section 3.2.2.1.2 or by the unannounced removal of power. The IPU and PCU shall not be damaged by the simultaneous turn-on of both the A-side and B-side spacecraft bus inputs. The PCU shall not be damaged by the shorting of any secondary power output line to ground. The IPU shall not be damaged by the shorting of any supply line to ground.

#### 3.2.2.1.5 PCU-IPU Power Interface Diagram

The PCU to IPU power interconnections are shown in Figure 3.2.2.1.5-1.

### 3.2.2.2 PCU-SPU Power Interface

#### 3.2.2.2.1 PCU Power to SPU

The PCU-to-SPU outputs of +5.5 Vdc ,+15 Vdc, and –15 Vdc shall come from converters within the PCU that are dedicated to the SPU and are switched by command from the IPU. The configuration of returns for these power outputs and their isolation and grounding shall conform to the requirements in SP-HIR-169.

At the inputs to the SPU, the power characteristics provided in Table 3.2.2.2.1-1 shall be met:

**Table 3.2.2.2.1-1 PCU to SPU Power Characteristics**

| | **5.5 V** | **+15 V** | **–15 V** |
|---|---|---|---|
| **Voltage limits at PCU end of cable** | +5.38 (TBR)<br>+5.62 (TBR) | +14.85<br>+15.25 | –14.85<br>–15.25 |
| **Voltage limits at SPU end of cable** | +5.28<br>+5.62 | +14.65<br>+15.25 | –14.75<br>–15.25 |
| **SPU Nominal DC load current (mA) (1)** | 400 | 840 | 370 |
| **Maximum resistance of cable + connector pins** | 150 mΩ | 150 mΩ | 150 mΩ |
| **Regulation:** | <50 mV | < 20 mV | < 20 mV |
| **PCU-induced ripple at PCU end of cable** | < 40 mVpp (2) | < 25 mVpp (3) | < 25 mVpp (3) |
| **Minimum Voltage Rise Time** | 380µs | 600µs | 700µs |

(1) 2-orbit average
(2) 10 Hz to 10 MHz, 200 mV max spikes at switching frequency
(3) 10 Hz to 10 MHz, 100 mV max spikes at switching frequency

### 3.2.2.2.2 SPU EOL Inputs

Table 3.2.2.2.2-2 show a breakdown of SPU maximum EOL current consumption under the assumption of one side failed shorted.

**Table 3.2.2.2.2-2 SPU Maximum EOL Current Consumption**

| Item | +5.5 Vdc mA | +15 Vdc mA | –15 Vdc mA |
|---|---|---|---|
| Nominal Operational Consumption | 400 | 840 | 370 |
| Current Limiter | 100 | 100 | 100 |
| EOL Allowance | 60 | 260 | 60 |
| Minimum PCU Current Requirement | 560 | 1200 | 530 |

### 3.2.2.2.3 Inrush

The PCU shall perform to all requirements when connected to the SPU having the capability of sinking inrush currents as shown in Figures 3.2.2.2.3-1 through 3.2.2.2.3-4.

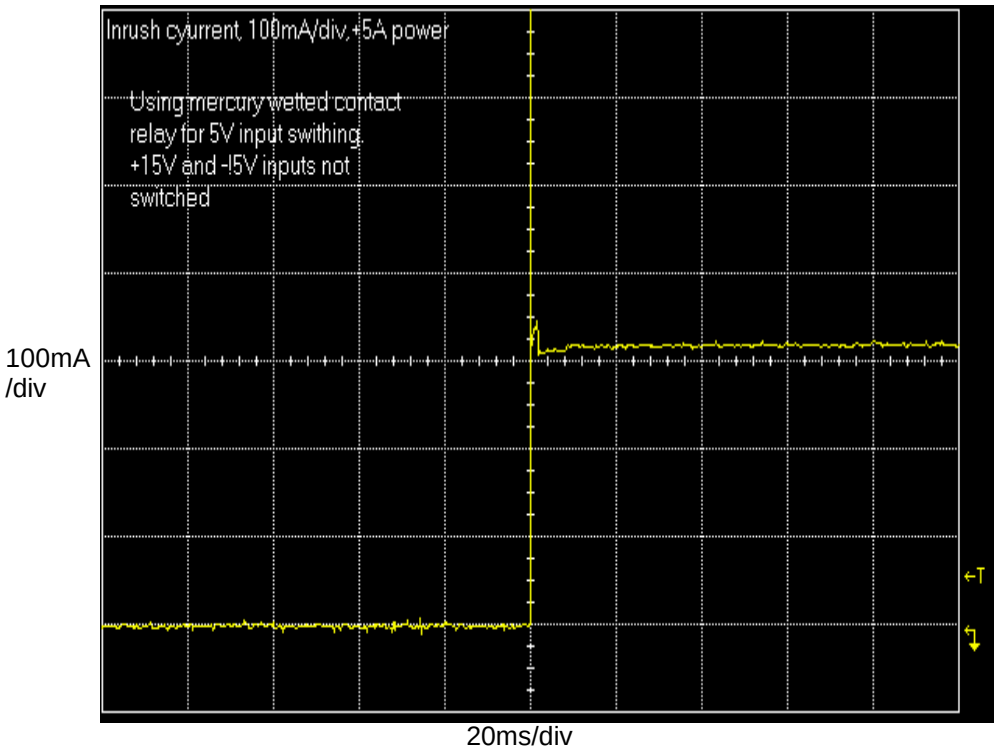


**Figure 3.2.2.2.3-1. SPU 5V Inrush when driven by an Ideal Power Supply.**

Vertical Scale: 100mA/div.; Horizontal Scale: 20ms/div.; Peak Current: ~320mA.

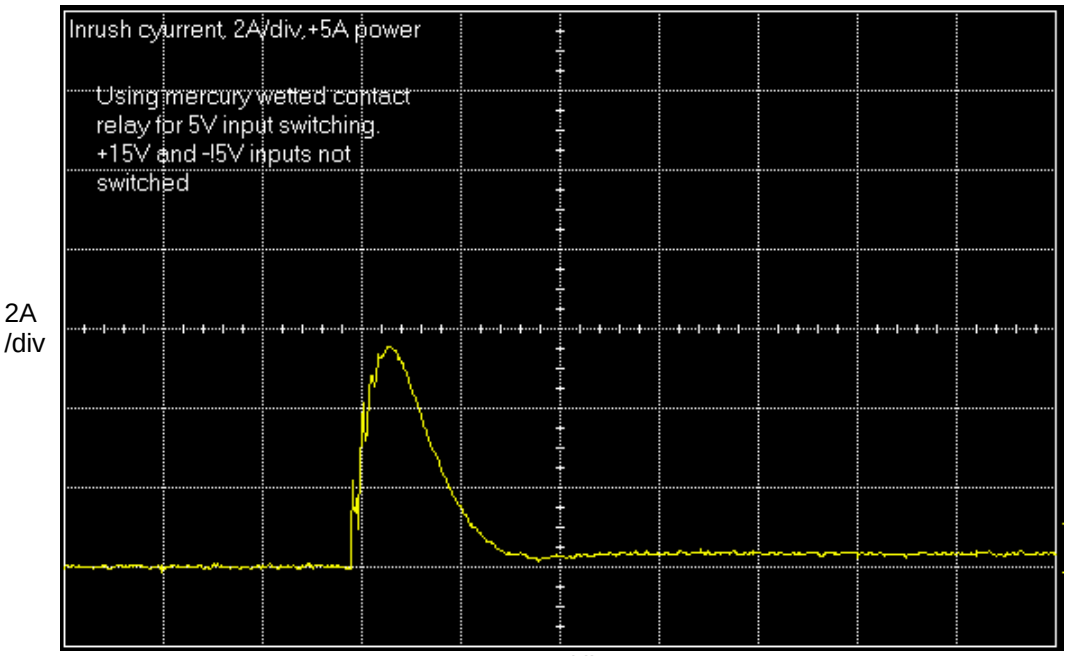


**Figure 3.2.2.2.3-2. SPU 5V Inrush When Driven by an Ideal Power Supply**

Vertical Scale: 2A/div.; Horizontal Scale: 200µs/div.; Peak Current: ~5.5A.

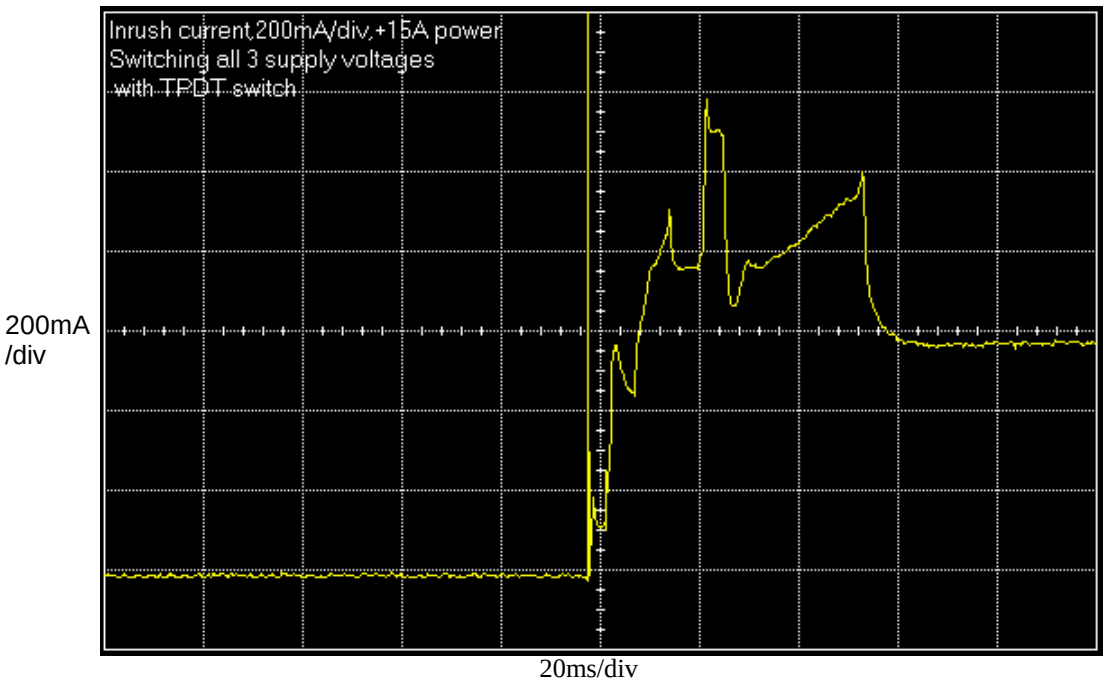


**Figure 3.2.2.2.3-3 SPU +15V Inrush When Driven by an Ideal Power Supply**

Vertical Scale: 200mA/div.; Horizontal Scale: 20ms/div.; Peak Current: ~1.2A.

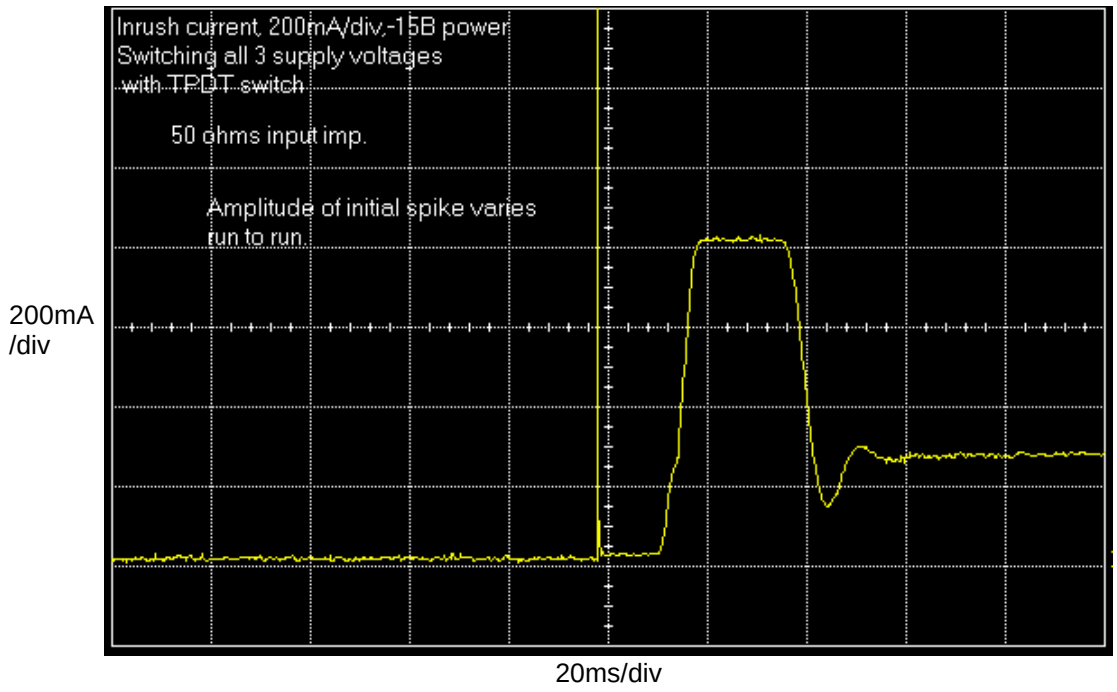


**Figure 3.2.2.2.3-4. SPU -15V Inrush when driven by an Ideal Power Supply**
Vertical Scale: 200mA/div.; Horizontal Scale: 20ms/div.; Peak Current: ~0.8 A.

### 3.2.2.2.4 SPU Fault Tolerance

The SPU shall not be damaged by the unannounced removal of power. The SPU shall not be damaged by the grounding of any of its inputs. The PCU shall not be damaged by the shorting of any output line to ground.

### 3.2.2.2.5 PCU-SPU Interface Characteristics

The PCU to SPU power interconnections are shown in Figure 3.2.2.2.5-1.

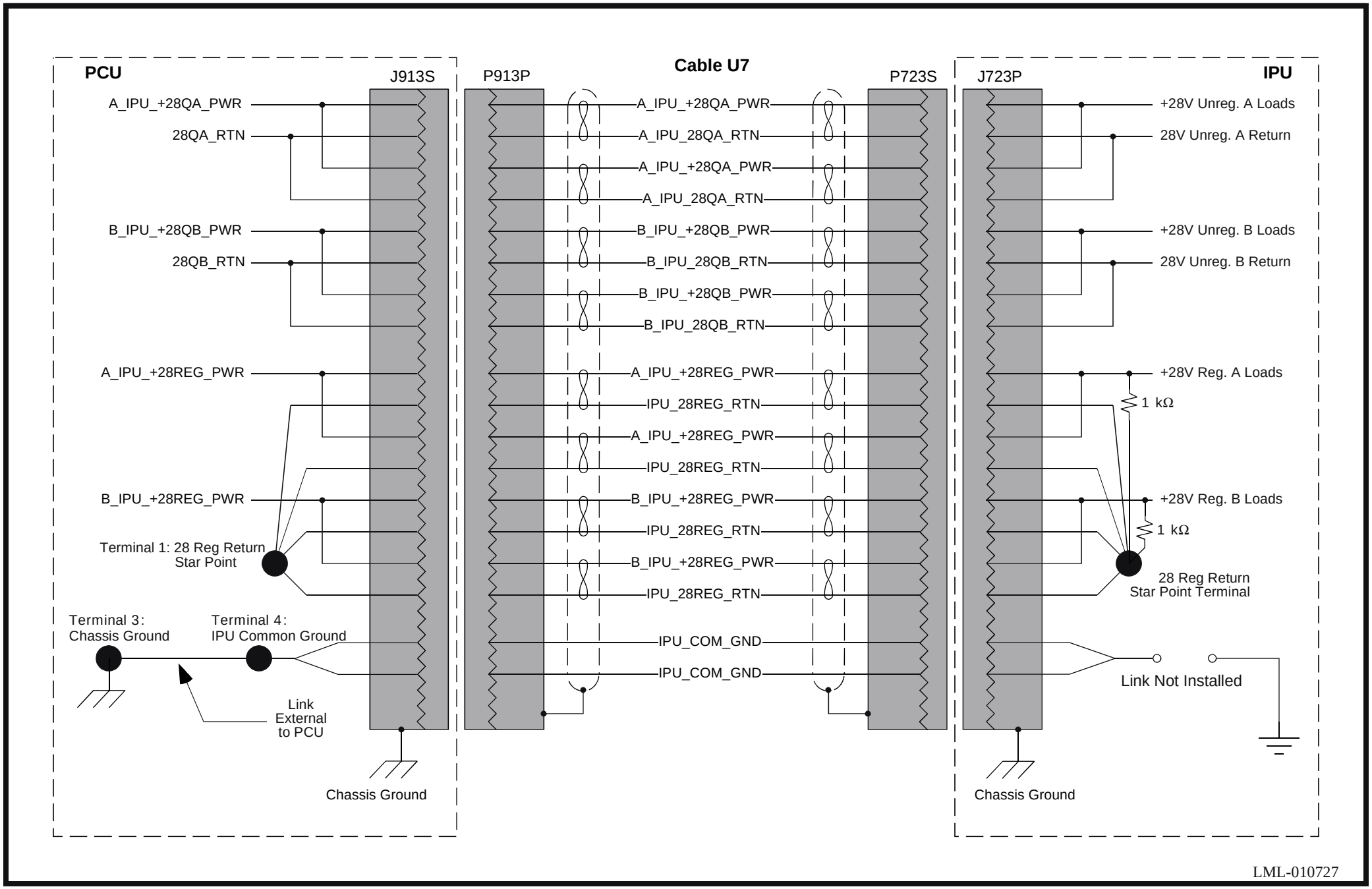


**Figure 3.2.2.1.5-1 PCU-IPU Power Interconnect**

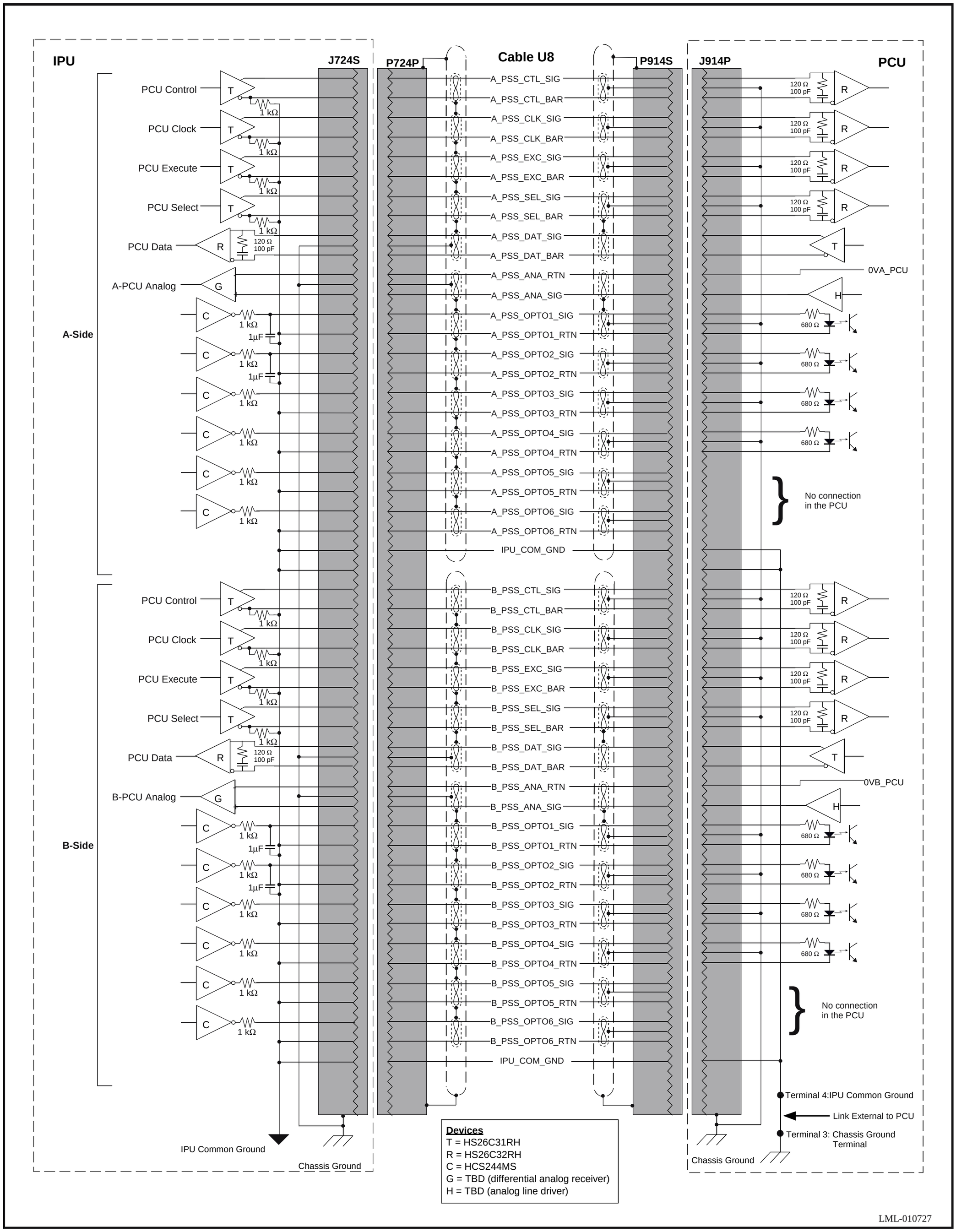


**Figure 3.2.3-1 IPU-PCU Control/Data Interconnections**

### 3.2.3 Control and Data Interface

The IPU to PCU digital control and data interface shall consist of six discrete drivers and five ANSI/TIA/EIA-422-B (RS-422) balanced voltage digital interface circuits on each side of the IPU (A side and B side). Each RS-422 circuit shall be terminated at the receiving end with a 120 Ω 5% resistor in series with a 100 pF 10% capacitor, connected across the inputs to the differential receiver as shown in Figure 3.2.3-1.

The control and data transfer shall be fully synchronous and all causal signals shall be defined as active low. The differential receiver circuits shall be fail safe to an output high for a high impedance input. Active low causal signals will therefore be inactive when an input is in a high impedance state. The differential driver outputs shall be a be defined as follows: a) logic one for a high level on the non-inverting output and a low level on the inverting output; b) logic zero for a low level on the non-inverting output and a high level on the inverting output. The differential receiver inputs shall be defined as: a) logic one for a high level on the non-inverting input and a low level on the inverting input. b) logic zero for a low level on the non-inverting input and a high level on the inverting input. The five serial control and data interface signals are listed in Table 3.2.3-1.

| Signal | Causal |
|---|---|
| PCU Clock | • |
| PCU Control | |
| PCU Select | • |
| PCU Execute | • |
| PCU Data | |

**Table 3.2.3-1 Digital Control & Data Signals**

Timing relationships between the signals of the Control and Data interface are shown in Figure 3.2.3–2 and are described in the following subsections.

#### 3.2.3.1 PCU Clock

The IPU shall output to the PCU a 20 kHz gated clock signal. This clock shall act as the synchronization signal for the serial control transfer from the IPU to the PCU and as the synchronization for the serial data transfer from the PCU to the IPU. The clock signal shall be active only while data are being transferred. This signal is active low (i.e. the active state is logic zero).

#### 3.2.3.2 PCU Control

The PCU Control line shall be used to define the following:

a. the state of all power-switching relays in the PCU except those controlled by discrete drive signals as defined in Section 3.2.3.6
b. which analog telemetry signal is to be presented on the Analog Data line by the PCU
c. which status word is to be presented to be transmitted on the PCU Data line

Section 3.3.X contains a detailed definition of the PCU control words.

This line shall be a 16 bit serial data line from the IPU to the PCU. The IPU shall change the control bits on the low-to-high (active to inactive) transition (trailing edge)of the clock and the PCU shall read the control bits on the high-to-low (inactive to active) transition (leading edge) of the clock. The most significant bit shall be sent first. Control data will be transferred to the PCU while the “Select” line is high (inactive) and while the “Execute” line is high (inactive). This signal is active high (i.e. a zero control bit is logic zero).

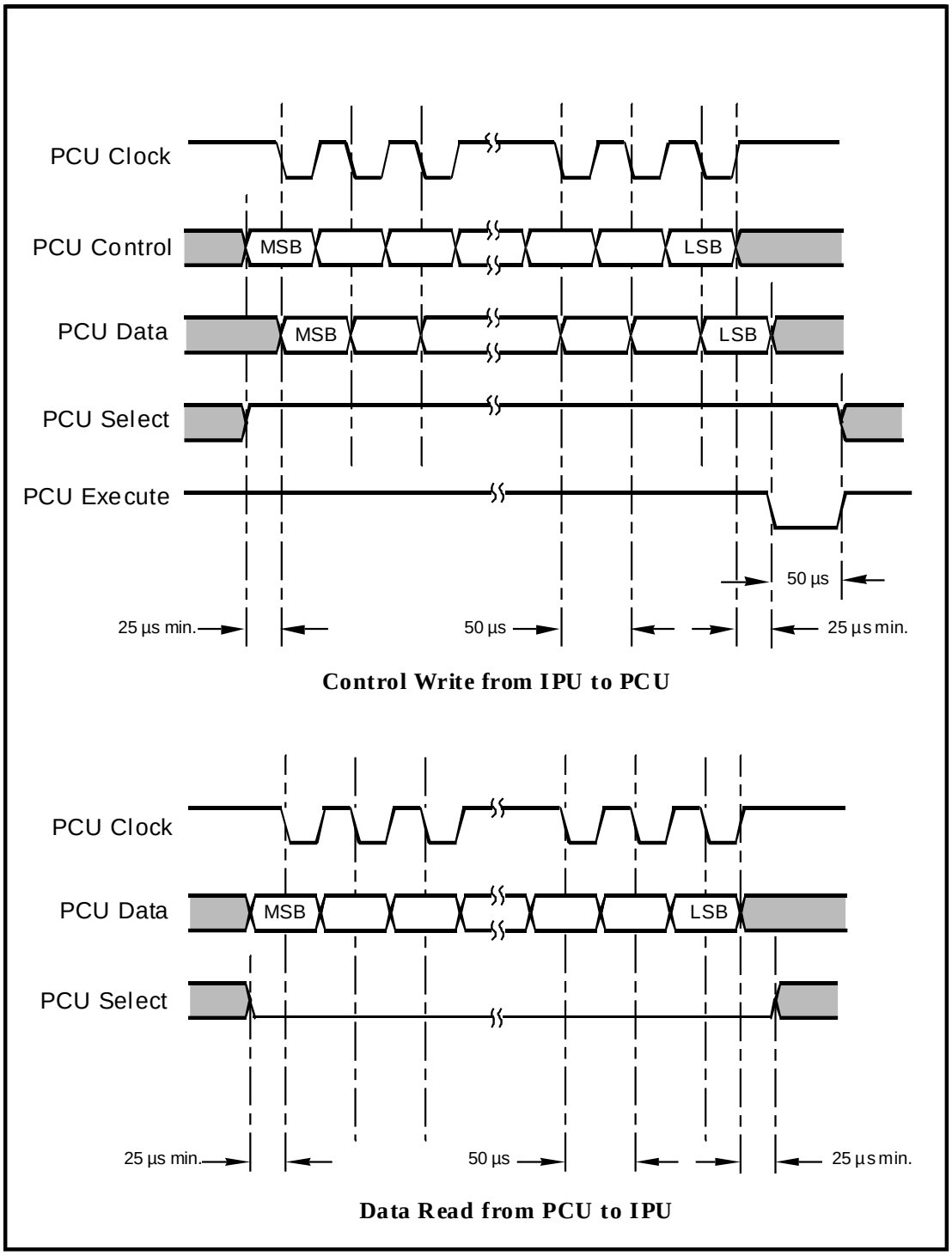


**Figure 3.2.3-2 IPU-PCU Control/Data Timing**

#### 3.2.3.3 PCU Select

The PCU Select line shall be used to define which type of data is to be transferred: a) control data from the IPU to the PCU and control echo from the PCU to IPU; or b) status data from the PCU to the IPU. If the Select line is high (inactive) the control data shall be transmitted synchronous with the clock from the IPU to the PCU and the output of the first stage of the serial input register shall be placed on the PCU Data line. If the select line is low (active) the status data shall be transmitted synchronous with the clock from the PCU to the IPU. The select line shall be valid at least one half clock cycle prior to the commencement of data transfer. This signal is active low (i.e. the active state is logic zero).

#### 3.2.3.4 PCU Execute

The PCU Execute line shall cause the current control word (the last 16 bits received on the PCU Control line) to be executed. The execute line is normally high (inactive) and will be set low (active) by the IPU for one clock period. This signal is active low (i.e. the active state is logic zero).

#### 3.2.3.5 PCU Data

The PCU Data line is used to confirm the PCU has received the proper control word prior to execution, and to transfer status data from the PCU to the IPU. When the select line is high (inactive), the PCU shall echo to the IPU the bit contained in the first stage of the serial control input register via the PCU Data line. The PCU shall change the echo bit on the high-to-low clock transition (leading edge). NOTE: The echo bit on the PCU Data line is required to change on the opposite clock edge from that on which the data bit must change during a Data Read sequence. The IPU shall read the echo bit on the low-to-high clock transition (trailing edge).

When the select line is low (active), The PCU shall transmit status data to the IPU. The PCU shall place the first bit of status data on the PCU Data line in response to the Select line going low (active). The PCU shall clock out status bits on the low to high transition (trailing edge) of the PCU Clock, and the IPU shall read the status bits on the high-to low transition (leading edge) of the PCU Clock. NOTE: This signal is active high (i.e. a zero control bit is logic zero).

#### 3.2.3.6 Discrete Drivers

The IPU shall provide a maximum of 12 drivers (6 from the A side and 6 from the B side) for opto-couplers in the PCU. Each driver shall consist of a Harris HCS244 buffer with a 1 kΩ series resistor.

### 3.2.4 Analog Signals

The PCU shall drive two (A-side and B-side) single-ended “Analog Data” lines with voltages representing various parameters within the PCU. These lines shall be driven with voltages in the range of ±10 Vdc. Which parameter is multiplexed onto these lines shall be controlled via a serial control word transmitted from the IPU to the PCU. Both the A and B-side lines shall be driven at the same time and with the same analog parameter..

### 3.2.5 Physical Electrical Interface

The electrical interface between the PCU and IPU consists of cables U7 and U8. The electrical interface between the PCU and SPU consists of cable U17.

#### 3.2.5.1 Connector Type Definitions

Connectors hard mounted on boxes or the structure are referred to as “jacks” (or “receptacles”) and will have the letter “J” preceding the connector number. Connectors located on harnesses, cables or wires will be referred to as “plugs” and will have the letter “P” preceding the connector number. The letter “S” or “P” at the end of the connector number specifies contact type: “S” for socket and “P” for pin.

Connector types used for the IPS-PSS electrical interfaces are defined in Table 3.2.5.1-1.

**Table 3.2.5.1-1 Connector Types**

| Jack No. | Location | PPL-21 Type | Pins | Plug No. | PPL-21 Type | Cable |
|---|---|---|---|---|---|---|
| J913S | PCU | 311P409-3S-B12 | 25 | P913P | 311P409-3P-B12 | U7 |
| J723P | IPU | 311P409-3P-B12 | 25 | P723S | 311P409-3S-B12 | U7 |
| J724S | IPU | 311P407-5S-B12 | 78 | P724P | 311P407-5P-B12 | U8 |
| J914P | PCU | 311P407-5P-B12 | 78 | P914S | 311P407-5S-B12 | U8 |
| J915S | PCU | 311P409-2S-B12 | 15 | P915P | 311P409-2P-B12 | U17 |
| J713P | SPU | 311P409-2P-B12 | 15 | P713S | 311P409-2S-B12 | U17 |

### 3.2.5.2 Connector Pinout Definitions

Signal names and pin assignments for Cables U7 (PCU to IPU Power), U8 (PCU-IPU Control/Data), and U17 (PCU to SPU Power) are defined in Tables 3.2.5.2-1 through 3.2.5.2-3.

**Table 3.2.5.2-1 Cable U7 (PCU to IPU Power)**

| **PCU** | | | | | | | **IPU** | |
|---|---|---|---|---|---|---|---|---|
| P913P | <————**Cable U7** ————> | | | | | | P723S | |
| J913S | <———**Box Receptacles**———> | | | | | | J723P | |
| PIN | SIGNAL NAME | TYPE | Vmax V | Imax mA | GROUP | WIRE TYPE | PIN | FUNCTION |
| 1 | Blank | | | | | | 13 | Blank |
| 2 | A_IPU_+28QA_PWR | Power | 36 | 2000 | T2-1A | ** | 12 | Unregulated +28V Power Side A |
| 3 | A_IPU_+28QA_PWR | Power | 36 | 2000 | T2-2A | ** | 11 | Unregulated +28V Power Side A |
| 4 | B_IPU_+28QB_PWR | Power | 36 | 2000 | T2-3A | ** | 10 | Unregulated +28V Power Side B |
| 5 | B_IPU_+28QB_PWR | Power | 36 | 2000 | T2-4A | ** | 9 | Unregulated +28V Power Side B |
| 6 | Blank | | | | | | 8 | Blank |
| 7 | A_IPU_+28REG_PWR | Power | 28 | 2000 | T2-5A | ** | 7 | Regulated +28V Power Side A |
| 8 | A_IPU_+28REG_PWR | Power | 28 | 2000 | T2-6A | ** | 6 | Regulated +28V Power Side A |
| 9 | B_IPU_+28REG_PWR | Power | 28 | 2000 | T2-7A | ** | 5 | Regulated +28V Power Side B |
| 10 | B_IPU_+28REG_PWR | Power | 28 | 2000 | T2-8A | ** | 4 | Regulated +28V Power Side B |
| 11 | Blank | | | | | | 3 | Blank |
| 12 | IPU_COM_GND | Ground | | | T2-9A | ** | 2 | IPU Common Ground |
| 13 | Blank | | | | | | 1 | Blank |
| 14 | Blank | | | | | | 25 | Blank |
| 15 | A_IPU_28QA_RTN | Pwr Rtn | 36 | 2000 | T2-1B | ** | 24 | Unregulated +28V Power Side A Return |
| 16 | A_IPU_28QA_RTN | Pwr Rtn | 36 | 2000 | T2-2B | ** | 23 | Unregulated +28V Power Side A Return |
| 17 | B_IPU_28QB_RTN | Pwr Rtn | 36 | 2000 | T2-3B | ** | 22 | Unregulated +28V Power Side B Return |
| 18 | B_IPU_28QB_RTN | Pwr Rtn | 36 | 2000 | T2-4B | ** | 21 | Unregulated +28V Power Side B Return |
| 19 | Blank | | | | | | 20 | Blank |
| 20 | IPU_28REG_RTN | Pwr Rtn | 28 | 2000 | T2-5B | ** | 19 | Regulated +28V Power Return |
| 21 | IPU_28REG_RTN | Pwr Rtn | 28 | 2000 | T2-6B | ** | 18 | Regulated +28V Power Return |
| 22 | IPU_28REG_RTN | Pwr Rtn | 28 | 2000 | T2-7B | ** | 17 | Regulated +28V Power Return |
| 23 | IPU_28REG_RTN | Pwr Rtn | 28 | 2000 | T2-8B | ** | 16 | Regulated +28V Power Return |
| 24 | Blank | | | | | | 15 | Blank |
| 25 | IPU_COM_GND | Ground | | | T2-9B | ** | 14 | IPU Common Ground |
| shell | U7_CHASS_GND | Shield | | | | | shell | U7 Overall Cable shield to Chassis |
| | | | | | | | | |
| ** | M22759/33-22-9 | | | | | | | |

## Table 3.2.5.2-2 Cable U8 (PCU-IPU Control/Data)

| PCU | | | | | | | IPU | |
|---|---|---|---|---|---|---|---|---|
| P914S | <————Cable U8————> | | | | | | P724P | |
| J914P | <———Box Receptacles———> | | | | | | J724S | |
| PIN | SIGNAL NAME | TYPE | Vmax V | Imax mA | GROUP | WIRE TYPE | PIN | FUNCTION |
| 1 | A_PSS_CTL_SIG | RS-422 | 6 | 150 | TS2-1A | * | 1 | PCU Control True Side A |
| 2 | A_PSS_CTL_BAR | RS-422 | 6 | 150 | TS2-1B | * | 2 | PCU Control Complement Side A |
| 3 | A_PSS_CLK_SIG | RS-422 | 6 | 150 | TS2-2A | * | 3 | PCU Clock True Side A |
| 4 | A_PSS_CLK_BAR | RS-422 | 6 | 150 | TS2-2B | * | 4 | PCU Clock Complement Side A |
| 5 | A_PSS_EXC_SIG | RS-422 | 6 | 150 | TS2-3A | * | 5 | PCU Execute True Side A |
| 6 | A_PSS_EXC_BAR | RS-422 | 6 | 150 | TS2-3B | * | 6 | PCU Execute Complement Side A |
| 7 | A_PSS_SEL_SIG | RS-422 | 6 | 150 | TS2-4A | * | 7 | PCU Select True Side A |
| 8 | A_PSS_SEL_BAR | RS-422 | 6 | 150 | TS2-4B | * | 8 | PCU Select Complement Side A |
| 9 | A_PSS_DAT_SIG | RS-422 | 6 | 150 | TS2-5A | * | 9 | PCU Data True Side A |
| 10 | A_PSS_DAT_BAR | RS-422 | 6 | 150 | TS2-5B | * | 10 | PCU Data Complement Side A |
| 11 | B_PSS_CTL_SIG | RS-422 | 6 | 150 | TS2-13A | * | 11 | PCU Control True Side B |
| 12 | B_PSS_CTL_BAR | RS-422 | 6 | 150 | TS2-13B | * | 12 | PCU Control Complement Side B |
| 13 | B_PSS_CLK_SIG | RS-422 | 6 | 150 | TS2-14A | * | 13 | PCU Clock True Side B |
| 14 | B_PSS_CLK_BAR | RS-422 | 6 | 150 | TS2-14B | * | 14 | PCU Clock Complement Side B |
| 15 | B_PSS_EXC_SIG | RS-422 | 6 | 150 | TS2-15A | * | 15 | PCU Execute True Side B |
| 16 | B_PSS_EXC_BAR | RS-422 | 6 | 150 | TS2-15B | * | 16 | PCU Execute Complement Side B |
| 17 | B_PSS_SEL_SIG | RS-422 | 6 | 150 | TS2-16A | * | 17 | PCU Select True Side B |
| 18 | B_PSS_SEL_BAR | RS-422 | 6 | 150 | TS2-16B | * | 18 | PCU Select Complement Side B |
| 19 | B_PSS_DAT_SIG | RS-422 | 6 | 150 | TS2-17A | * | 19 | PCU Data True Side B |
| 20 | B_PSS_DAT_BAR | RS-422 | 6 | 150 | TS2-17B | * | 20 | PCU Data Complement Side B |
| 21 | A_PSS_CTL_SHD | Shield | | | | | | PCU Control Cable Shield |
| 22 | A_PSS_ANA_SHD | Shield | | | | | | PCU Analog Cable Shield |
| 23 | A_PSS_CLK_SHD | Shield | | | | | | PCU Clock Cable Shield |
| 24 | A_PSS_OPTO1_SHD | Shield | | | | | | PCU Opto Cable Shield |
| 25 | A_PSS_EXC_SHD | Shield | | | | | | PCU Execute Cable Shield |
| 26 | A_PSS_OPTO2_SHD | Shield | | | | | | PCU Opto Cable Shield |
| 27 | A_PSS_SEL_SHD | Shield | | | | | | PCU Select Cable Shield |
| 28 | A_PSS_OPTO3_SHD | Shield | | | | | | PCU Opto Cable Shield |
| 29 | A_PSS_DAT_SHD | Shield | | | | | | PCU Data Cable Shield |
| 30 | Blank | | | | | | 30 | Blank |
| 31 | B_PSS_CTL_SHD | Shield | | | | | | PCU Control Cable Shield |
| 32 | B_PSS_OPTO1_SHD | Shield | | | | | | PCU Opto Cable Shield |
| 33 | B_PSS_CLK_SHD | Shield | | | | | | PCU Clock Cable Shield |
| 34 | B_PSS_OPTO2_SHD | Shield | | | | | | PCU Opto Cable Shield |
| 35 | B_PSS_EXC_SHD | Shield | | | | | | PCU Execute Cable Shield |
| 36 | B_PSS_OPTO3_SHD | Shield | | | | | | PCU Opto Cable Shield |
| 37 | B_PSS_SEL_SHD | Shield | | | | | | PCU Select Cable Shield |
| 38 | B_PSS_ANA_SHD | Shield | | | | | | PCU Analog Cable Shield |
| 39 | B_PSS_DAT_SHD | Shield | | | | | | PCU Data Cable Shield |
| 40 | Blank | | | | | | 40 | Blank |

| **PCU** | | | | | | | **IPU** | |
|---|---|---|---|---|---|---|---|---|
| P914S | <————**Cable U8**————> | | | | | | P724P | |
| J914P | <———**Box Receptacles**———> | | | | | | J724S | |
| PIN | SIGNAL NAME | TYPE | Vmax V | Imax mA | GROUP | WIRE TYPE | PIN | FUNCTION |
| 41 | A_PSS_ANA_SIG | Analog | 15 | | TS2-6A | * | 41 | PCU Analog Side A |
| 42 | A_PSS_ANA_RTN | An Rtn | 0 | 0 | TS2-6B | * | 42 | PCU Analog Return Side A |
| 43 | A_PSS_OPTO1_SIG | Pulse | 3.5 | 2 | TS2-7A | * | 43 | PCU Opto-coupler 1 Signal Side A |
| 44 | A_PSS_OPTO1_RTN | Pulse | 0 | 2 | TS2-7B | * | 44 | PCU Opto-coupler 1 Return |
| 45 | A_PSS_OPTO2_SIG | Pulse | 3.5 | 2 | TS2-8A | * | 45 | PCU Opto-coupler 2 Signal Side A |
| 46 | A_PSS_OPTO2_RTN | Pulse | 0 | 2 | TS2-8B | * | 46 | PCU Opto-coupler 2 Return |
| 47 | A_PSS_OPTO3_SIG | Pulse | 3.5 | 2 | TS2-9A | * | 47 | PCU Opto-coupler 3 Signal Side A |
| 48 | A_PSS_OPTO3_RTN | Pulse | 0 | 2 | TS2-9B | * | 48 | PCU Opto-coupler 3 Return |
| 49 | IPU_COM_GND | Ground | 0 | 0 | | ** | 49 | Signal Ground |
| 50 | IPU_COM_GND | Ground | 0 | 0 | | ** | 50 | Signal Ground |
| 51 | B_PSS_OPTO1_SIG | Pulse | 3.5 | 2 | TS2-18A | * | 51 | PCU Opto-coupler 1 Signal Side B |
| 52 | B_PSS_OPTO1_RTN | Pulse | 0 | 2 | TS2-18B | * | 52 | PCU Opto-coupler 1 Return Side B |
| 53 | B_PSS_OPTO2_SIG | Pulse | 3.5 | 2 | TS2-19A | * | 53 | PCU Opto-coupler 2 Signal Side B |
| 54 | B_PSS_OPTO2_RTN | Pulse | 0 | 2 | TS2-19B | * | 54 | PCU Opto-coupler 2 Return Side B |
| 55 | B_PSS_OPTO3_SIG | Pulse | 3.5 | 2 | TS2-20A | * | 55 | PCU Opto-coupler 3 Signal Side B |
| 56 | B_PSS_OPTO3_RTN | Pulse | 0 | 2 | TS2-20B | * | 56 | PCU Opto-coupler 3 Return Side B |
| 57 | B_PSS_ANA_SIG | Analog | 15 | | TS2-21A | * | 57 | PCU Analog Side B |
| 58 | B_PSS_ANA_RTN | An Rtn | 0 | 0 | TS2-21B | * | 58 | PCU Analog Return Side B |
| 59 | Blank | | | | | | 59 | Blank |
| 60 | A_PSS_OPTO4_SHD | Shield | | | | | | PCU Opto Cable Shield |
| 61 | A_PSS_OPTO4_SIG | Pulse | 3.5 | 2 | TS2-10A | * | 61 | PCU Opto-coupler 4 Signal Side A |
| 62 | A_PSS_OPTO4_RTN | Pulse | 0 | 2 | TS2-10B | * | 62 | PCU Opto-coupler 4 Return |
| 63 | A_PSS_OPTO5_SHD | Shield | | | | | | No connection in PCU |
| 64 | A_PSS_OPTO5_SIG | Pulse | 3.5 | 2 | TS2-11A | * | 64 | No connection in PCU |
| 65 | A_PSS_OPTO5_RTN | Pulse | 0 | 2 | TS2-11B | * | 65 | No connection in PCU |
| 66 | A_PSS_OPTO6_SHD | Shield | | | | | | No connection in PCU |
| 67 | A_PSS_OPTO6_SIG | Pulse | 3.5 | 2 | TS2-12A | * | 67 | No connection in PCU |
| 68 | A_PSS_OPTO6_RTN | Pulse | 0 | 2 | TS2-12B | * | 68 | No connection in PCU |
| 69 | Blank | | | | | | 69 | Blank |
| 70 | B_PSS_OPTO4_SIG | Pulse | 3.5 | 2 | TS2-22A | * | 70 | PCU Opto-coupler 4 Signal Side A |
| 71 | B_PSS_OPTO4_RTN | Pulse | 0 | 2 | TS2-22B | * | 71 | PCU Opto-coupler 4 Return |
| 72 | B_PSS_OPTO4_SHD | Shield | | | | | | PCU Opto Cable Shield |
| 73 | B_PSS_OPTO5_SIG | Pulse | 3.5 | 2 | TS2-23A | * | 73 | No connection in PCU |
| 74 | B_PSS_OPTO5_RTN | Pulse | 0 | 2 | TS2-23B | * | 74 | No connection in PCU |
| 75 | B_PSS_OPTO5_SHD | Shield | | | | | | No connection in PCU |
| 76 | B_PSS_OPTO6_SIG | Pulse | 3.5 | 2 | TS2-24A | * | 76 | No connection in PCU |
| 77 | B_PSS_OPTO6_RTN | Pulse | 0 | 2 | TS2-24B | * | 77 | No connection in PCU |
| 78 | B_PSS_OPTO6_SHD | Shield | | | | | | No connection in PCU |
| shell | PSS_CHASS_GND | Shield | | | | | shell | Cable U8 Overall Shield to Chassis |
| | | | | | | | | |
| * | M27500-24SC2S23 | | | | | | | |
| ** | M22759/33-22-9 | | | | | | | |

**Table 3.2.5.2-3 Cable U17 (PCU to SPU Power)**

| **SPU** | | | | | | | **PCU** | |
|---|---|---|---|---|---|---|---|---|
| P713S | <————**Cable U17**————> | | | | | | P915P | |
| J713P | <———**Box Receptacles**———> | | | | | | J915S | |
| PIN | SIGNAL NAME | TYPE | Vmax V | Imax mA | GROUP | WIRE TYPE | PIN | FUNCTION |
| | | | | | | | | |
| 1 | SPU_+5B_PWR | Power | 6 | 600 | TS4-1A | * | 1 | SPU +5V Power Side B |
| 2 | SPU_5_SHD | Shield | | | | | 2 | SPU 5V Shield |
| 3 | SPU_+5A_PWR | Power | 6 | 600 | TS4-1B | * | 3 | SPU +5V Power Side A |
| 4 | Blank | | | | | | 4 | Blank |
| 5 | SPU_15A_RTN | Pwr Rtn | 0 | 1800 | TS6-1A | ** | 5 | SPU 15V Power Return Side A |
| 6 | SPU_15_SHD | Shield | | | | | 6 | SPU 15V Shield |
| 7 | SPU_+15B_PWR | Power | 15 | 1200 | TS6-1B | ** | 7 | SPU +15V Power Side B |
| 8 | SPU_–15B_PWR | Power | –15 | 600 | TS6-1C | ** | 8 | SPU –15V Power Side B |
| 9 | SPU_5B_RTN | Pwr Rtn | 0 | 600 | TS4-1C | * | 9 | SPU +5V Power Return Side B |
| 10 | SPU_5A_RTN | Pwr Rtn | 0 | 600 | TS4-1D | * | 10 | SPU +5V Power Return Side A |
| 11 | SPU_COM_GND | Ground | | | | ** | 11 | SPU Common Ground |
| 12 | SPU_+15A_PWR | Power | 15 | 1200 | TS6-1D | ** | 12 | SPU +15V Power Side A |
| 13 | SPU_–15A_PWR | Power | –15 | 600 | TS6-1E | ** | 13 | SPU –15V Power Side A |
| 14 | SPU_COM_GND | Ground | | | | ** | 14 | SPU Common Ground |
| 15 | SPU_15B_RTN | Pwr Rtn | 0 | 1800 | TS6-1F | ** | 15 | SPU 15V Power Return Side B |
| shell | U17_CHASS_GND | Shield | | | | | shell | U17 Overall Shield to Chassis |
| | | | | | | | | |
| * | M27500-22SC4S23 | | | | | | | |
| ** | M22759/33-22-9 | | | | | | | |

## 3.3 Functional Interface

### 3.3.1 IPU Control Words

The IPU shall transmit a continuous sequence of Data Request Word (DRW) codes, each corresponding to a specific PCU telemetry function. Two types of PCU telemetry data are requested by a DRW - Analog Data (temperature and voltage) and Digital Data (relay status).

#### 3.3.1.1 IPU Digital Data Request

Each Digital Data Request from the IPU to the PCU shall be a 16-bit serial word, transmitted MSB-first. Table 3.3.1.1-1 lists each Digital Data function, the corresponding digital DRW hex code, and shows how each function is mapped onto the Instrument Telemetry List.

**Table 3.3.1.1-1 Digital Data Request Codes and Telemetry List Mapping**

| DATA WORD BIT | BIT DEFINITION | | |
|---|---|---|---|
| **4000** | **PSS_STATUS_00** | | |
| 0 | A_IPU +28REG supply redt. relay OFF/ON | Logic 1 = Relay ON | b |
| 1 | A_IPU +28REG supply prim. relay OFF/ON | Logic 1 = Relay ON | a |
| 2 | +28REG supply to A_IPU OFF/ON | Logic 1 indicates that IPU A is supplied with +28Volts | |
| 3 | B_IPU +28REG supply redt. relay OFF/ON | Logic 1 = Relay ON | b, x |
| 4 | B_IPU +28REG supply prim. relay OFF/ON | Logic 1 = Relay ON | a, x |
| 5 | +28REG supply to B_IPU OFF/ON | Logic 1 indicates that IPU B is supplied with +28Volts | x |
| 6 | Logic 0 | Input to the 4000 Buffer grounded | x |
| 7 | Logic 0 | Input to the 4000 Buffer grounded | |
| 8 | GND | Permanent Logic 0 | |
| 9 | +5A power to SPU OFF/ON | Logic 1 = Relay ON; SPU_+5A_PWR ON | x |
| 10 | +15A power to SPU OFF/ON | Logic 1 = Relay ON; SPU_+15A_PWR ON | x |
| 11 | -15A power to SPU OFF/ON | Logic 1 = Relay ON; SPU_-15A_PWR ON | x |
| 12 | +5V SYS Converter A input OFF/ON | Logic 1 = Primary Power supplied | |
| 13 | +5V SYS Converter B input OFF/ON | Logic 1 = Primary Power supplied | |
| 14 | +28REG SYS Converter A input OFF/ON | Logic 1 = Primary Power supplied | |
| 15 | +28REG SYS Converter B input OFF/ON | Logic 1 = Primary Power supplied | |
| **4001** | **PSS_STATUS_01** | | |
| 0 | A_TEU +5V supply redt. relay OFF/ON | Logic 1 = Relay ON | b |
| 1 | A_TEU +5V supply prim. relay OFF/ON | Logic 1 = Relay ON | a |
| 2 | +5V supply to A_TEU OFF/ON | Logic 1 indicates that TEU A is supplied with +5Volts | |
| 3 | A_TEU +/-15V supply redt. relay OFF/ON | Logic 1 = Relay ON | d, x |
| 4 | A_TEU +/-15V supply prim. relay OFF/ON | Logic 1 = Relay ON | c, x |
| 5 | +15V supply to A_TEU OFF/ON | Logic 1 indicates that TEU A is supplied with +15Volts | x |
| 6 | -15V supply to A_TEU OFF/ON | Logic 1 indicates that TEU A is supplied with -15Volts | x |
| 7 | Logic 0 | Input to the 4001 Buffer grounded | x |

| DATA WORD BIT | BIT DEFINITION | | |
|---|---|---|---|
| 8 | GND | Permanent Logic 0 | |
| 9 | Logic 0 | Input to the 4001 Buffer grounded | |
| 10 | Logic 0 | Input to the 4001 Buffer grounded | |
| 11 | Logic 0 | Input to the 4001 Buffer grounded | |
| 12 | +15V SYS Converter A input OFF/ON | Logic 1 = Primary Power supplied | |
| 13 | +15V SYS Converter B input OFF/ON | Logic 1 = Primary Power supplied | |
| 14 | -15V SYS Converter A input OFF/ON | Logic 1 = Primary Power supplied | |
| 15 | -15V SYS Converter B input OFF/ON | Logic 1 = Primary Power supplied | |
| **4002** | **PSS_STATUS_02** | | |
| 0 | GSS +5V supply redt. relay OFF/ON | Logic 1 = Relay ON | b |
| 1 | GSS +5V supply prim. relay OFF/ON | Logic 1 = Relay ON | a |
| 2 | +5V supply to GSS OFF/ON | Logic 1 indicates that GSS is supplied with +5Volts | |
| 3 | GSS +/-15V supply redt. relay OFF/ON | Logic 1 = Relay ON | d, x |
| 4 | GSS +/-15V supply prim. relay OFF/ON | Logic 1 = Relay ON | c, x |
| 5 | +15V supply to GSS OFF/ON | Logic 1 indicates that GSS is supplied with +15Volts | x |
| 6 | -15V supply to GSS OFF/ON | Logic 1 indicates that GSS is supplied with -15Volts | x |
| 7 | Logic 0 | Input to the 4002 Buffer grounded | x |
| 8 | GND | Permanent Logic 0 | |
| 9 | +5B power to SPU OFF/ON | Logic 1 = Relay ON; SPU_+5B_PWR ON | x |
| 10 | +15B power to SPU OFF/ON | Logic 1 = Relay ON; SPU_+15B_PWR ON | x |
| 11 | -15B power to SPU OFF/ON | Logic 1 = Relay ON; SPU_-15B_PWR ON | x |
| 12 | PCU Internal Converter A OFF/ON | Logic 1 = Primary Power supplied | |
| 13 | PCU Internal Converter B OFF/ON | Logic 1 = Primary Power supplied | |
| 14 | SPU A Converters OFF/ON | Logic 1 = Primary Power supplied | |
| 15 | SPU B Converters OFF/ON | Logic 1 = Primary Power supplied | |
| **4003** | **PSS_STATUS_03** | | |
| 0 | +28NA redt. relay OFF/ON | Logic 1 = Relay ON; 28NA_RTN is switched | e |
| 1 | +28NA prim. relay OFF/ON | Logic 1 = Relay ON; 28NA_RTN is switched | e |
| 2 | +28NC supply to CSS OFF/ON | Logic 1 indicates that CCS is supplied with Power | |
| 3 | Logic zero | Input to the 4003 Buffer grounded | x |
| 4 | Logic zero | Input to the 4003 Buffer grounded | |
| 5 | +28NB redt. relay OFF/ON | Logic 1 = Relay ON; 28NB_RTN is switched | f |
| 6 | +28NB prim. relay OFF/ON | Logic 1 = Relay ON; 28NB_RTN is switched | f |
| 7 | Logic zero | Input to the 4003 Buffer grounded | x |
| 8 | GND | Permanent Logic 0 | |
| 9-15 | Not used | Don’t care | |
| **4004** | **PSS_STATUS_04** | | |
| 0 | B_TEU +5 redt. relay OFF/ON | Logic 1 = Relay ON | b |
| 1 | B_TEU +5 prim. relay OFF/ON | Logic 1 = Relay ON | a |

| DATA WORD BIT | BIT DEFINITION | | |
|---|---|---|---|
| 2 | +5V supply to B_TEU OFF/ON | Logic 1 indicates that TEU B is supplied with +5Volts | |
| 3 | B_TEU +/-15 redt. relay OFF/ON | Logic 1 = Relay ON | d, x |
| 4 | B_TEU +/-15 prim. relay OFF/ON | Logic 1 = Relay ON | c, x |
| 5 | +15V supply to B_TEU OFF/ON | Logic 1 indicates that TEU B is supplied with +15Volts | x |
| 6 | -15V supply to B_TEU OFF/ON | Logic 1 indicates that TEU B is supplied with -15Volts | x |
| 7 | Logic zero | Input to the 4004 Buffer grounded | x |
| 8 | GND | Permanent Logic 0 | |
| 9-15 | Not used | Don't care | |
| **4005** | **PSS_STATUS_05** | | |
| 0 | EEA +5 redt. relay OFF/ON | Logic 1 = Relay ON | b |
| 1 | EEA +5 prim. relay OFF/ON | Logic 1 = Relay ON | a |
| 2 | +5V supply to EEA OFF/ON | Logic 1 indicates that EEA is supplied with +5Volts | |
| 3 | EEA +/-15 redt. relay OFF/ON | Logic 1 = Relay ON | d, x |
| 4 | EEA +/-15 prim. relay OFF/ON | Logic 1 = Relay ON | c, x |
| 5 | +15V supply to EEA OFF/ON | Logic 1 indicates that EEA is supplied with +15Volts | x |
| 6 | -15V supply to EEA OFF/ON | Logic 1 indicates that EEA is supplied with -15Volts | x |
| 7 | Logic zero | Input to the 4005 Buffer grounded | x |
| 8 | GND | Permanent Logic 0 | |
| 9-15 | Not used | Don't care | |
| **4006** | **PSS_STATUS_06** | | |
| 0 | A_TEU +28QC supply redt. relay OFF/ON | Logic 1 = Relay ON | g |
| 1 | A_TEU +28QC supply prim. relay OFF/ON | Logic 1 = Relay ON | g |
| 2 | 28QC supply to A_TEU OFF/ON | Logic 1 indicates that TEU A is supplied with Primary Power | |
| 3 | B_TEU +28QC supply redt. relay OFF/ON | Logic 1 = Relay ON | g, x |
| 4 | B_TEU +28QC supply prim. relay OFF/ON | Logic 1 = Relay ON | g, x |
| 5 | +28QC supply to B_TEU OFF/ON | Logic 1 indicates that TEU B is supplied with Primary Power | x |
| 6 | Logic 0 | Input to 4006 Buffer grounded | x |
| 7 | Logic 0 | Input to 4006 Buffer grounded | |
| 8 | GND | Permanent Logic 0 | x |
| 9-11 | not used | Don't care | |
| 12 | GSS +28QC supply redt. relay OFF/ON | Logic 1 = Relay ON | g, x |
| 13 | GSS +28QC supply prim. relay OFF/ON | Logic 1 = Relay ON | g, x |
| 14 | +28QC supply to GSS OFF/ON | Logic 1 indicates that GSS is supplied with Primary Power | x |
| 15 | +28QC internal bus below 20V | Logic 1 = +28QC Volts below 20Volts | x |
| **4007** | **PSS_STATUS_07** | | |
| 0 | +28QA (Prim) N/L relay OFF/ON | Logic 1 = Relay ON | |

| DATA WORD BIT | BIT DEFINITION | | |
|---|---|---|---|
| 1 | +28QA (Redt) N/L relay OFF/ON | Logic 1 = Relay ON | |
| 2 | +28QA S/C input power OFF/ON | Logic 1 indicates that the Primary Power is present | x |
| 3 | +28QB (Prim) N/L relay OFF/ON | Logic 1 = Relay ON | x |
| 4 | +28QB (Redt) N/L relay OFF/ON | Logic 1 = Relay ON | x |
| 5 | +28QB S/C input power OFF/ON | Logic 1 indicates that the Primary Power is present | x |
| 6 | +28QC internal bus OFF/ON | Logic 1 indicates that the +28QC Power is ON | x |
| 7 | Logic 0 | Input to Buffer 4007 grounded | x |
| 8 | GND | Permanent Logic 0 | x |
| 9 - 15 | not used | Don't Care | |

**Footnotes to above table**

a. Not valid unless +5V/+28REG SYS Converters **A** powered ON
b. Not valid unless +5V/+28REG SYS Converters **B** powered ON
c. Not valid unless +/-15V SYS Converters **A** powered ON
d. Not valid unless +/-15V SYS Converters **B** powered ON
e. Not valid unless S/C **NA** bus input powered ON
f. Not valid unless S/C **NB** bus input powered ON
g. Not valid unless +28QC internal bus powered ON
x. This Request/Word has been changed with respect to the Engineering Model PSS

### 3.3.1.2 IPU Analog Data Request

Each Analog Data Request from the IPU to the PCU shall be a 16-bit serial word, transmitted MSB-first. Table 3.3.1.2-1 lists each Analog Data function, the corresponding digital DRW hex code, and shows, for information only, how each function is mapped on to the Instrument Telemetry List. This table also provides the scaling factors for the PFM data. EM scaling factor are provided for information only.

**Table 3.3.1.2-1 Analog Data Request Codes and Telemetry List Mapping**

| ANALOG TELEMETRY FUNCTION | DRW HEX CODE | TELEMETRY LIST MNEMONIC | SCALING FACTORS | |
|---|---|---|---|---|
| | | | EM | PFM |
| QA Primary Current | 0006 | QA_CURRT | N/A | 0.5000 |
| QB Primary Current | 0007 | QB_CURRT | N/A | 0.5000 |
| Internal PCU +5V supply (com) | 0001 | PSS_PCU_5V | 0.9724 | 0.7986 |
| Internal PCU +15V supply (com) | 0002 | PSS_PCU_P15V | 0.4686 | 0.2717 |
| Internal PCU -15V supply (com) | 0003 | PSS_PCU_N15V | 0.4692 | 0.2732 |
| Internal PCU +5V supply (Aside) | 0004 | PSS_PCU_5VA | N/A | 0.7991 |
| Internal PCU +5V supply (Bside) | 0005 | PSS_PCU_5VB | N/A | 0.7987 |
| +5 DC-DC Converter Voltage SYS A | 0008 | PSS_SYS_5VA | 0.9586 | 0.7992 |
| +15 DC-DC Converter Voltage SYS A | 0009 | PSS_SYS_P15VA | 0.4663 | 0.2730 |
| -15 DC-DC Converter Voltage SYS A | 000A | PSS_SYS_N15VA | 0.4682 | 0.2731 |
| +28REG DC-DC Converter Voltage A | 000B | PSS_REG_28VA | 0.3084 | 0.1419 |

| | | | | |
|---|---|---|---|---|
| +5 DC-DC Converter Voltage SYS B | 000C | PSS_SYS_5VB | 0.9582 | 0.7991 |
| +15 DC-DC Converter Voltage SYS B | 000D | PSS_SYS_P15VB | 0.4672 | 0.2719 |
| -15 DC-DC Converter Voltage SYS B | 000E | PSS_SYS_N15VB | 0.4687 | 0.2735 |
| +28REG DC-DC Converter Voltage B | 000F | PSS_REG_28VB | 0.3088 | 0.1418 |
| +5 DC-DC Converter Voltage SPU A | 1001 | PSS_SPU_5VA | 0.9762 | 0.7081 |
| +15 DC-DC Converter Voltage SPU A | 1002 | PSS_SPU_P15VA | 0.4932 | 0.2047 |
| -15 DC-DC Converter Voltage SPU A | 1003 | PSS_SPU_N15VA | 0.4884 | 0.2059 |
| +5 DC-DC Converter Voltage SPU B | 1005 | PSS_SPU_5VB | N/A | 0.7069 |
| +15 DC-DC Converter Voltage SPU B | 1006 | PSS_SPU_P15VB | N/A | 0.2048 |
| -15 DC-DC Converter Voltage SPU B | 1007 | PSS_SPU_N15VB | N/A | 0.2059 |
| +/-15 V PCU A Converter temp. | 1008 | PSS_PCU_15VATMP | N/A | 10mV/K |
| +/-15V PCU B Converter temp. | 100C | PSS_PCU_15VBTMP | N/A | 10mV/K |
| +5 V SYS A Converter temp. | 2000 | PSS_SYS_5VATMP | N/A | 10mV/K |
| +15 V SYS A Converter temp. | 2001 | PSS_SYS_P15VATMP | N/A | 10mV/K |
| -15V SYS A Converter temp. | 2002 | PSS_SYS_N15VATMP | N/A | 10mV/K |
| +28 VREG A Converter temp. | 2003 | PSS_REG_28VATMP | N/A | 10mV/K |
| +5 V SYS B Converter temp. | 2004 | PSS_SYS_5VBTMP | N/A | 10mV/K |
| +15V SYS B Converter temp. | 2005 | PSS_SYS_P15VBTMP | N/A | 10mV/K |
| -15V SYS B Converter temp. | 2006 | PSS_SYS_N15VBTMP | N/A | 10mV/K |
| +28VREG B Converter temp. | 2007 | PSS_REG_28VBTMP | N/A | 10mV/K |
| +5 V SPU A Converter temp. | 1009 | PSS_SPU_5VATMP | N/A | 10mV/K |
| +15 V SPU A Converter temp. | 100A | PSS_SPU_P15VATMP | N/A | 10mV/K |
| -15 V SPU A Converter temp. | 100B | PSS_SPU_N15VATMP | N/A | 10mV/K |
| +5V SPU B Converter temp. | 100D | PSS_SPU_5VBTMP | N/A | 10mV/K |
| +15 V SPU B Converter temp. | 100E | PSS_SPU_P15VBTMP | N/A | 10mV/K |
| -15 V SPU B Converter temp. | 100F | PSS_SPU_N15VBTMP | N/A | 10mV/K |
| QA Transient Limiter temp (1) | 200A | PSS_QAFILT_TMP | N/A | 10mV/K |
| QB Transient Limiter temp (1) | 200B | PSS_QBFILT_TMP | N/A | 10mV/K |
| +28QA prim. N/L relay temp. | 200C | PSS_QAP_RLY_TMP | N/A | 10mV/K |
| +28QA redt. N/L relay temp. | 200D | PSS_QAR_RLY_TMP | N/A | 10mV/K |
| +28QB prim. N/L relay temp. | 200E | PSS_QBP_RLY_TMP | N/A | 10mV/K |
| +28QB redt. N/L relay temp. | 200F | PSS_QBR_RLY_TMP | N/A | 10mV/K |

(1) Combined with QA/QB current sensor temp. monitor

### 3.3.2 PCU Data Words

The PCU shall transfer telemetry data to the IPU on request from the IPU. Immediately following each DRW, the PCU shall make available the corresponding data channel.

#### 3.3.2.1 PCU Digital Data Words

For each Data Word bit:

0 indicates Off, Inhibited, A-side or Primary side as applicable;
1 indicates On, Enabled, B-side or Redundant side as applicable.

Each PCU Digital Data Word shall be 16 bits, transmitted serially to the IPU, MSB-first. Each word shall consist of individual relay status bits as defined in Table 3.3.1.1-1. Each bit of the Telemetry List Word corresponds to the same PCU-IPU Data Word bit. Note - some status bits are invalid in certain conditions. See relevant note for details.

#### 3.3.2.2 PCU Analog Data Words

Analog telemetry functions and corresponding telemetry list mnemonics are listed in Table 3.3.1.2-1. Analog data shall be multiplexed, but not digitized, within the PCU. All analog data shall be digitized to 8-bit (or better) accuracy by the IPU. Data shall be valid after a delay of 10 ms following the end of a DRW.

### 3.3.3 Discrete Pulses from IPU to PSS

The command HIR_PSS_DISCRETE shall be used to change the cross-strapping configuration between the PCU "internal" converters and the Quiet Bus inputs. The default configuration is A-to-A, B-to-B, and does not need to be changed except for testing or in the event of a malfunction.

The HIR_PSS_DISCRETE command shall have a single parameter (#0) with the values and functions shown in Table 3.3.3-1. According to the value of Parameter #0, the IPU shall generate a 48 ms pulse routed to the appropriate PCU relay coils. **Note**:- the "RL" column refers to the relay number in the PCU as given on the RAL relay switching, command and telemetry schematic for the PCU.

**Table 3.3.3-1 HIR_PSS_DISCRETE Command Functions**

| PARAM #0 VALUE | RL # | FUNCTION |
|---|---|---|
| 1 | 53/ 54 | Connect PCU Internal Supply A to QBA;<br>Connect PCU Internal Supply B to QBB. |
| 2 | 53/ 54 | Connect PCU Internal Supply A to QBB;<br>Connect PCU Internal Supply B to QBA. |

Command verification status depends on which Quiet Bus line is powered, according to the following truth table:-

**Table 3.3.3-2 HIR_PSS_DISCRETE Command Verification Truth Table**

| PARAM #0 VALUE | QUIET BUS STATUS | PSS_STATUS_02 | |
|---|---|---|---|
| | | BIT #12 | BIT #13 |
| 1 | QA ON | 1 | 0 |
| 1 | QB ON | 0 | 1 |
| 2 | QA ON | 0 | 1 |
| 2 | QB ON | 1 | 0 |

### 3.3.4 Individual Relay Control (IRC) Words

Each IRC Word from the IPU to the PCU shall be 16 bits, transmitted MSB-first. Consecutive IRCs shall have a minimum interval between them of 45 ms. IRCs D00A, D00B, F00A and F00B require not less than 100ms interval before next IRC is sent.

**Table 3.3.4-1 Individual Relay Control (IRC) Codes &Telemetry Verification**

| Individual Relay Control Function | RL # | IRC HEX CODE | Used In PWR Switching Macro # | Verification TLM ( PSS_STATUS_XX) Mnemonic, Bit |
|---|---|---|---|---|
| Internal +28QA Power Bus & Return (prim) ON [non-latching relay] | 1 | F00A | 58 | _07, 0 = 1 AND _07, 2 = 1 AND _06, 15 = 1 AND _07, 6 = 1 |
| Internal +28QA Power Bus & Return (prim) ON [non-latching relay] | 2 | D00A | 59 | _07, 1 = 1 AND _07, 2 = 1 AND _06, 15 = 1 AND _07, 6 = 1 |
| Internal +28QB Power Bus & Return (prim) ON [non-latching relay] | 3 | F00B | 60 | _07, 3 = 1 AND _07, 5 = 1 AND _06, 15 = 1 AND _07, 6 = 1 |
| Internal +28QB Power Bus & Return (prim) ON [non-latching relay] | 4 | D00B | 61 | _07, 4 = 1 AND _07, 5 = 1 AND _06, 15 = 1 AND _07, 6 = 1 |
| NA & Return (prim) Select | 43 | F01C | 04 | _03, 1 = 1 AND _03, 2 = 1 |
| NA & Return(prim) Deselect | | E01C | 03, 05, 07, 08 | _03, 1 = 0 AND _03, 2 = 0 |
| NA & Return (redt) Select | 44 | D01C | 05 | _03, 0 = 1 AND _03, 2 = 1 |
| NA & Return (redt) Deselect | | C01C | 03, 04, 07, 08 | _03, 0 = 0 AND _03, 2 = 0 |
| NB & Return (prim) Select | 45 | F01D | 07 | _03, 2 = 1 AND _03, 6 = 1 |
| NB & Return (prim) Deselect | | E01D | 04, 05, 06, 08 | _03, 2 = 0 AND _03, 6 = 0 |
| NB & Return (redt) Select | 46 | D01D | 08 | _03, 2 = 1 AND _03, 5 = 1 |
| NB & Return (redt) Deselect | | C01D | 04, 05, 06, 07 | _03, 2 = 0 AND _03, 5 = 0 |
| SPU +5 V & +/-15 V (Conv. A) ON | 47 | B005 | 10 | _02, 14 = 1 |
| SPU +5 V & +/-15 V (Conv. A) OFF | | A005 | 01, 12, 62 | _02, 14 = 0 |
| SPU +5 V & +/-15 V (Conv. B) ON | 50 | 9005 | 12 | _02, 15 = 1 |
| SPU +5 V & +/-15 V (Conv. B) OFF | | 8005 | 01, 10, 63 | _02, 15 = 0 |
| SYS +5V, +28 VREG (Conv. A) ON | 19 | B001 | 13 | _00, 12 = 1 AND _00, 14 = 1 |
| SYS +5V, +28 VREG (Conv. A) OFF | | A001 | 01, 14, 64 | _00, 12 = 0 AND _00, 14 = 0 |
| SYS +5V, +28 VREG (Conv. B) ON | 20 | 9001 | 14 | _00, 13 = 1 AND _00, 15 = 1 |
| SYS +5V, +28 VREG (Conv. B) OFF | | 8001 | 01, 13, 65 | _00, 13 = 0 AND _00, 15 = 0 |
| SYS +15 V & -15 V (Conv. A) ON | 21 | B002 | 15 | _01, 12 = 1 AND _01, 14 = 1 |
| SYS +15 V & -15 V (Conv. A) OFF | | A002 | 01, 16, 66 | _01, 12 = 0 AND _01, 14 = 0 |

| Individual Relay Control Function | RL # | IRC HEX CODE | Used In PWR Switching Macro # | Verification TLM ( PSS_STATUS_ XX) Mnemonic, Bit |
|---|---|---|---|---|
| SYS +15 V & -15 V (Conv. B) ON | 22 | 9002 | 16 | _01, 13 = 1 AND _01, 15 = 1 |
| SYS +15 V & -15 V (Conv. B) OFF | | 8002 | 01, 15, 67 | _01, 13 = 0 AND _01, 15 = 0 |
| TEU A (prim) +28Q ON | 13 | F014 | 18 | _06, 1 = 1 AND _06, 2 = 1 |
| TEU A (prim) +28Q OFF | | E014 | 02, 17, 19, 21, 22 | _06, 1 = 0 AND _06, 2 = 0 |
| TEU A (redt) +28Q ON | 14 | D014 | 19 | _06, 0 = 1 AND _06, 2 = 1 |
| TEU A (redt) +28Q OFF | | C014 | 02, 17, 18, 21, 22 | _06, 0 = 0 AND _06, 2 = 0 |
| TEU B (prim) +28Q ON | 15 | F015 | 21 | _06, 4 = 1 AND _06, 5 = 1 |
| TEU B (prim) +28Q OFF | | E015 | 02, 18, 19, 20, 22 | _06, 4 = 0 AND _06, 5 = 0 |
| TEU B (redt) +28Q ON | 16 | D015 | 22 | _06, 3 = 1 AND _06, 5 = 1 |
| TEU B (redt) +28Q OFF | | C015 | 02, 18, 19, 20, 21 | _06, 3 = 0 AND _06, 5 = 0 |
| IPU (A Side) +28REG (prim) ON | 23 | F002 | 24 | _00, 1 = 1 AND _00, 2 = 1 |
| IPU (A Side) +28REG (prim) OFF | | E002 | 02, 23, 25, 27, 28 | _00, 1 = 0 AND _00, 2 = 0 |
| IPU (A Side) +28REG (redt) ON | 24 | D002 | 25 | _00, 0 = 1 AND _00, 2 = 1 |
| IPU (A Side) +28REG (redt) OFF | | C002 | 02, 23, 24, 27, 28 | _00, 0 = 0 AND _00, 2 = 0 |
| IPU (B Side) +28REG (prim) ON | 25 | F003 | 27 | _00, 4 = 1 AND _00, 5 = 1 |
| IPU (B Side) +28REG (prim) OFF | | E003 | 02, 24, 25, 26, 28 | _00, 4 = 0 AND _00, 5 = 0 |
| IPU (B Side) +28REG (redt) ON | 26 | D003 | 28 | _00, 3 = 1 AND _00, 5 = 1 |
| IPU (B Side) +28REG (redt) OFF | | C003 | 02, 24, 25, 26, 27 | _00, 3 = 0 AND _00, 5 = 0 |
| GSS +28Q (prim) ON | 17 | F016 | 30 | _06, 13 = 1 AND _06, 14 = 1 |
| GSS +28Q (prim) OFF | | E016 | 02, 29, 31 | _06, 13 = 0 AND _06, 14 = 0 |
| GSS +28Q (redt) ON | 18 | D016 | 31 | _06, 12 = 1 AND _06, 14 = 1 |
| GSS +28Q (redt) OFF | | C016 | 02, 29, 30 | _06, 12 = 0 AND _06, 14 = 0 |
| GSS +5 V (prim) ON | 27 | F004 | 33, 34 | _02, 1 = 1 AND _02, 2 = 1 |
| GSS +5 V (prim) OFF | | E004 | 02, 32, 35, 36 | _02, 1 = 0 AND _02, 2 = 0 |
| GSS +5 V (redt) ON | 28 | D004 | 35, 36 | _02, 0 = 1 AND _02, 2 = 1 |
| GSS +5 V (redt) OFF | | C004 | 02, 32, 33, 34 | _02, 0 = 0 AND _02, 2 = 0 |
| GSS +/-15 V (prim) ON | 29 | F005 | 33, 35 | _02, 4 = 1 AND _02, 5 = 1 AND _02, 6 = 1 |
| GSS +/-15 V (prim) OFF | | E005 | 02, 32, 34, 36 | _02, 4 = 0 AND _02, 5 = 0 AND _02, 6 = 0 |
| GSS +/-15 V (redt) ON | 30 | D005 | 34, 36 | _02, 3 = 1 AND _02, 5 = 1 AND _02, 6 = 1 |
| GSS +/-15 V (redt) OFF | | C005 | 02, 32, 33, 35 | _02, 3 = 0 AND _02, 5 = 0 AND _02, 6 = 0 |
| SPU A +5 V ON | 48 | F018 | 38 | _00, 9 = 1 |
| SPU A +5 V OFF | | E018 | 02, 37, 40 | _00, 9 = 0 |
| SPU B +5 V ON | 51 | D018 | 40 | _02, 9 = 1 |
| SPU B +5 V OFF | | C018 | 02, 38, 39 | _02, 9 = 0 |
| SPU A +15 V & -15 V ON | 49 | F019 | 38 | _00, 10 = 1 AND _00, 11 = 1 |
| SPU A +15 V & -15 V OFF | | E019 | 02, 37, 40 | _00, 10 = 0 AND _00, 11 = 0 |
| SPU B +15 V & -15 V ON | 52 | D019 | 40 | _02, 10 = 1 AND _02, 11 = 1 |
| SPU B +15 V & -15 V OFF | | C019 | 02, 38, 39 | _02, 10 = 0 AND _02, 11 = 0 |
| TEU A +5 V (prim) ON | 35 | F00C | 42 | _01, 1 = 1 AND _01, 2 = 1 |
| TEU A +5 V (prim) OFF | | E00C | 02, 41, 43, 48, 49, 51, 52 | _01, 1 = 0 AND _01, 2 = 0 |
| TEU A +5 V (redt) ON | 36 | D00C | 43 | _01, 0 = 1 AND _01, 2 = 1 |
| TEU A +5 V (redt) OFF | | C00C | 02, 41, 42, 48, 49, 51, 52 | _01, 0 = 0 AND _01, 2 = 0 |
| TEU A +15 V & -15 V (prim) ON | 39 | F00D | 45 | _01, 4 = 1 AND _01, 5 = 1 AND _01, 6 = 1 |
| TEU A +15 V & -15 V (prim) OFF | | E00D | 02, 44, 46, 48, 49, 51, 52 | _01, 4 = 0 AND _01, 5 = 0 AND _01, 6 = 0 |
| TEU A +15 V & -15 V (redt) ON | 40 | D00D | 46 | _01, 3 = 1 AND _01, 5 = 1 AND _01, 6 = 1 |

| Individual Relay Control Function | RL # | IRC HEX CODE | Used In PWR Switching Macro # | Verification TLM ( PSS_STATUS_ XX) Mnemonic, Bit |
|---|---|---|---|---|
| TEU A +15 V & -15 V (redt) OFF | | C00D | 02, 44, 45, 48, 49, 51, 52 | _01, 3 = 0 AND _01, 5 = 0 AND _01, 6 = 0 |
| TEU B +5 V (prim) ON | 37 | F010 | 48 | _04, 1 = 1 AND _04, 2 = 1 |
| TEU B +5 V (prim) OFF | | E010 | 02, 42, 43, 46, 47, 49 | _04, 1 = 0 AND _04, 2 = 0 |
| TEU B +5 V (redt) ON | 38 | D010 | 49 | _04, 0 = 1 AND _04, 2 = 1 |
| TEU B +5 V (redt) OFF | | C010 | 02, 42, 43, 45, 46, 47, 48 | _04, 0 = 0 AND _04, 2 = 0 |
| TEU B +15 V & -15 V (prim) ON | 41 | F011 | 51 | _04, 4 = 1 AND _04, 5 = 1 AND _04, 6 = 1 |
| TEU B +15 V & -15 V (prim) OFF | | E011 | 50 | _04, 4 = 0 AND _04, 5 = 0 AND _04, 6 = |
| TEU B +15 V & -15 V (redt) ON | 42 | D011 | 52 | _04, 3 = 1 AND _04, 5 = 1 AND _04, 6 = 1 |
| TEU B +15 V & -15 V (redt) OFF | | C011 | 02, 42, 43, 45, 46, 50, 51 | _04, 3 = 0 AND _04, 5 = 0 AND _04, 6 = 0 |
| EEA +5 V (prim) ON | 31 | F008 | 54, 55 | _05, 1 = 1 AND _05, 2 = 1 |
| EEA +5 V (prim) OFF | | E008 | 02, 53, 56, 57 | _05, 1 = 0 AND _05, 2 = 0 |
| EEA +5 V (redt) ON | 32 | D008 | 56, 57 | _05, 0 = 1 AND _05, 2 = 1 |
| EEA +5 V (redt) OFF | | C008 | 02, 53, 54, 55 | _05, 0 = 0 AND _05, 2 = 0 |
| EEA +15 V & -15 V (prim) ON | 33 | F009 | 54, 56 | _05, 4 = 1 AND _05, 5 = 1 AND _05, 6 = 1 |
| EEA +15 V & -15 V (prim) OFF | | E009 | 02, 53, 55, 57 | _05, 4 = 0 AND _05, 5 = 0 AND _05, 6 = 0 |
| EEA +15 V & -15 V (redt) ON | 34 | D009 | 55, 57 | _05, 3 = 1 AND _05, 5 = 1 AND _05, 6 = |
| EEA +15 V & -15 V (redt) OFF | | C009 | 02, 53, 54, 56 | _05, 3 = 0 AND _05, 5 = 0 AND _05, 6 = 0 |

### 3.3.5 PSS Function Codes & PSM Code Sequences

PSS Function Codes (PFC) have been assigned to each of the switching functions shown in Fig. 2 of document SP-HIR-169 "HIRDLS Power Distribution, Switching & Grounding". Parameters of the command HIR_PSS_SWITCH correspond to each of these PCU power switching functions. Each PFC has been assigned two command parameters. The first parameter identifies the function and the second parameter defines the required final state of the associated switch(es).

In most cases, a power-switching operation requires two or more IRCs to be transmitted from the IPU to the PCU in a predetermined sequence which includes time delays. These sequences have been implemented as Power Switching Macros (PSM) within the IPU. Table 3.3.5-1 defines the PSM and IRC Hex Code sequence to be sent to the PCU on receipt by the IPU of a given PFC. The right hand column shows the telemetry verification status on completion of the macro.

## Table 3.3.5-1 PFCs , PSMs and IRC Hex Code Sequences **

| PFC | PSM # | SWITCHING FUNCTION | IRC CODE SEQUENCE | Verification TLM (PSS_STATUS_ XX) Mnemonic, Bit |
|---|---|---|---|---|
| 08, 0 | PSM-01 | Reset Conv Input Relays to OFF | 8005-A005-8002-A002-8001-A001 | No meaningful verification possible |
| 09, 0 | PSM-02 | Reset Load Pwr Relays to OFF | C019-C018-E019-E018-C016-E016-C005-C004-E005-E004-C009-C008-E009-E008-C011-C00D-E011-E00D-C010-C00C-E010-E00C-E014-C014-E015-C015-E002-C002-E003-C003-E01C-C01C-E01D-C01D | No meaningful verification possible<br>(NOTE: red commands added since previous release) |
| 10,1 | PSM-58 | Prim. Int. +28QA Bus On | F00A (Note 1) | _07, 0 = 1 AND _07, 2 = 1 AND _06, 15 = 1 AND _07, 6 = 1 |
| 11,1 | PSM-59 | Redt. Int. +28QA Bus On | D00A (Note 1) | _07, 1 = 1 AND _07, 2 = 1 AND _06, 15 = 1 AND _07, 6 = 1 |
| 12,1 | PSM-60 | Prim. Int. +28QB Bus On | F00B (Note 1) | _07, 3 = 1 AND _07, 5 = 1 AND _06, 15 = 1 AND _07, 6 = 1 |
| 13,1 | PSM-61 | Redt. Int. +28QB Bus On | D00B (Note 1) | _07, 4 = 1 AND _07, 5 = 1 AND _06, 15 = 1 AND _07, 6 = 1 |
| 18, 0 | PSM-03 | CSS Inhibit Pwr from Noisy Bus A (prim & redt) | E01C-C01C | _03, 0 = 0 AND _03, 1 = 0 AND _03, 2 = 0 |
| 18, 1 | PSM-04 | CSS Enable Pwr from Noisy Bus A (prim) | E01D-C01D-C01C-F01C | _03, 0 = 0 AND _03, 1 = 1 AND _03, 2 = 1 |
| 18, 2 | PSM-05 | CSS Enable Pwr from Noisy Bus A (redt) | E01D-C01D-E01C-D01C | _03, 0 = 1 AND _03, 1 = 0 AND _03, 2 = 1 |
| 19, 0 | PSM-06 | CSS Inhibit Pwr from Noisy Bus B (prim & redt) | E01D-C01D | 03, 2 = 0 AND _03, 5 = 0 AND _03, 6 = 0 |
| 19, 1 | PSM-07 | CSS Enable Pwr from Noisy Bus B (prim) | E01C-C01C-C01D-F01D | 03, 2 = 1 AND _03, 5 = 0 AND _03, 6 = 1 |
| | | | | |
| 19, 2 | PSM-08 | CSS Enable Pwr from Noisy Bus B (redt) | E01C-C01C-E01D-D01D | 03, 2 = 1 AND _03, 5 = 1 AND _03, 6 = 0 |
| 22, 0 | PSM-62 | SPU +5/±15 Conv Gp A OFF | A005 | _02, 14 = 0 |
| 22, 1 | PSM-10 | SPU +5/±15 Conv Gp A ON | 8005 - B005 | _02, 14 = 1 |
| 23, 0 | PSM-63 | SPU +5/±15 Conv Gp B OFF | 8005 | _02, 15 = 0 |
| 23, 1 | PSM-12 | SPU +5/±15 Conv Gp B ON | A005 - 9005 | _02, 15 = 1 |
| 26, 0 | PSM-64 | SYS +5/+28 Conv Gp A OFF | A001 | _00, 12 = 0 AND _00, 14 = 0 |
| 26, 1 | PSM-13 | SYS +5/+28 Conv Gp A ON | 8001 - B001 | _00, 12 = 1 AND _00, 14 = 1 |
| 27, 0 | PSM-65 | SYS +5/+28 Conv Gp B OFF | 8001 | _00, 13 = 0 AND _00, 15 = 0 |
| 27, 1 | PSM-14 | SYS +5/+28 Conv Gp B ON | A001 - 9001 | _00, 13 = 1 AND _00, 15 = 1 |
| 28, 0 | PSM-66 | SYS ±15 Conv Gp A OFF | A002 | _01, 12 = 0 AND _01, 14 = 0 |

| PFC | PSM # | SWITCHING FUNCTION | IRC CODE SEQUENCE | Verification TLM (PSS_STATUS_ XX) Mnemonic, Bit |
|---|---|---|---|---|
| 28, 1 | PSM-15 | SYS ±15 Conv Gp A ON | 8002 - B002 | _01, 12 = 1 AND _01, 14 = 1 |
| 29, 0 | PSM-67 | SYS±15 Conv Gp B OFF | 8002 | _01, 13 = 0 AND _01, 15 = 0 |
| 29, 1 | PSM-16 | SYS ±15 Conv Gp B ON | A002 - 9002 | _01, 13 = 1 AND _01, 15 = 1 |
| 35, 0 | PSM-17 | +28Q Supply to A_TEU OFF | E014 - C014 | _06, 0 = 0 AND _06, 1 = 0 AND _06, 2 = 0 |
| 35, 1 | PSM-18 | +28Q Supply to A_TEU ON (prim) | E015 - C015 - C014 - F014 | _06, 0 = 0 AND _06, 1 = 1 AND _06, 2 = 1 |
| 35, 2 | PSM-19 | +28Q Supply to A_TEU ON (redt) | E015 - C015 - E014 - D014 | _06, 0 = 1 AND _06, 1 = 0 AND _06, 2 = 1 |
| 36, 0 | PSM-20 | +28Q Supply to B_TEU OFF | E015 - C015 | _06, 3 = 0 AND _06, 4 = 0 AND _06, 5 = 0 |
| 36, 1 | PSM-21 | +28Q Supply to B_TEU ON (prim) | E014 - C014 - C015 - F015 | _06, 3 = 0 AND _06, 4 = 1 AND _06, 5 = 1 |
| 36, 2 | PSM-22 | +28Q Supply to B_TEU ON (redt) | E014 - C014 - E015 - D015 | _06, 3 = 1 AND _06, 4 = 0 AND _06, 5 = 1 |
| 40, 0 | PSM-23 | +28REG Supply to A_IPU OFF | E002 - C002 | _00, 0 = 0 AND _00, 1 = 0 AND _00, 2 = 0 |
| 40, 1 | PSM-24 | +28REG Supply to A_IPU ON (prim) | E003 - C003 - C002 - F002 | _00, 0 = 0 AND _00, 1 = 1 AND _00, 2 = 1 |
| 40, 2 | PSM-25 | +28REG Supply to A_IPU ON (redt) | E003 - C003 - E002 - D002 | _00, 0 = 1 AND _00, 1 = 0 AND _00, 2 = 1 |
| 41, 0 | PSM-26 | +28REG Supply to B_IPU OFF | E003 - C003 | _00, 3 = 0 AND _00, 4 = 0 AND _00, 5 = 0 |
| 41, 1 | PSM-27 | +28REG Supply to B_IPU ON (prim) | E002 - C002 - C003 - F003 | _00, 3 = 0 AND _00, 4 = 1 AND _00, 5 = 1 |
| 41, 2 | PSM-28 | +28REG Supply to B_IPU ON (redt) | E002 - C002 - E003 - D003 | _00, 3 = 1 AND _00, 4 = 0 AND _00, 5 = 1 |
| 42, 0 | PSM-29 | +28Q Supply to GSS OFF | E016 - C016 | _06, 12 = 0 AND _06, 13 = 0 AND _06, 14 = 0 |
| 42, 1 | PSM-30 | +28Q Supply to GSS ON (prim) | C016 - F016 | _06, 12 = 0 AND _06, 13 = 1 AND _06, 14 = 1 |
| 42, 2 | PSM-31 | +28Q Supply to GSS ON (redt) | E016 - D016 | _06, 12 = 1 AND _06, 13 = 0 AND _06, 14 = 1 |
| 43, 0 | PSM-32 | +5/±15 Supplies to GSS OFF | E005 - C005 - E004 - C004 | _02, 0 = 0 AND _02, 1 = 0 AND _02, 2 = 0 AND _02, 3 = 0 AND _02, 4 = 0 AND _02, 5 = 0 AND _02, 6 = 0 |
| 43, 1 | PSM-33 | +5/±15 Supplies to GSS ON (prim) | C004 - C005 - F004 - F005 | _02, 0 = 0 AND _02, 1 = 1 AND _02, 2 = 1 AND _02, 3 = 0 AND _02, 4 = 1 AND _02, 5 = 1 AND _02, 6 = 1 |
| 43, 2 | PSM-34 | +5/±15 Supplies to GSS ON (5 prim, 15 redt) | C004 - E005 - F004 - D005 | _02, 0 = 0 AND _02, 1 = 1 AND _02, 2 = 1 AND _02, 3 = 1 AND _02, 4 = 0 AND _02, 5 = 1 AND _02, 6 = 1 |
| 43, 3 | PSM-35 | +5/±15 Supplies to GSS ON (5 redt, 15 prim) | E004 - C005 - D004 - F005 | _02, 0 = 1 AND _02, 1 = 0 AND _02, 2 = 1 AND _02, 3 = 0 AND _02, 4 = 1 AND _02, 5 = 1 AND _02, 6 = 1 |
| 43, 4 | PSM-36 | +5/±15 Supplies to GSS ON (5 redt, 15 redt) | E004 - E005 - D004 - D005 | _02, 0 = 1 AND _02, 1 = 0 AND _02, 2 = 1 AND _02, 3 = 1 AND _02, 4 = 0 AND _02, 5 = 1 AND _02, 6 = 1 |
| 44, 0 | PSM-37 | +5/±15 A-side Supplies to SPU OFF | E018 - E019 | _00, 9 = 0 AND _00, 10 = 0 AND _00, 11 = 0 |
| 44, 1 | PSM-38 | +5/±15 A-side Supplies to SPU ON | C018 - C019 - F019 - F018 | _00, 9 = 1 AND _00, 10 = 1 AND _00, 11 = 1 |
| 45, 0 | PSM-39 | +5/±15 B-side Supplies to SPU OFF | C018 - C019 | _02, 9 = 0 AND _02, 10 = 0 AND _02, 11 = 0 |
| 45, 1 | PSM-40 | +5/±15 B-side Supplies to SPU ON | E018 - E019 - D019 - D018 | _02, 9 = 1 AND _02, 10 = 1 AND _02, 11 = 1 |
| 46, 0 | PSM-41 | +5 Supplies to TEU A-side OFF | E00C - C00C | _01, 1 = 0 AND _01, 2 = 0 AND _01, 0 = 0 |
| 46, 1 | PSM-42 | +5 Supplies to TEU A-side ON (prim) | C00C - E010 - C010 - F00C | _01, 1 = 1 AND _01, 2 = 1 |
| 46, 2 | PSM-43 | +5 Supplies to TEU A-side ON (redt) | E00C - E010 - C010 - D00C | _01, 0 = 1 AND _01, 2 = 1 |

| PFC | PSM # | SWITCHING FUNCTION | IRC CODE SEQUENCE | Verification TLM (PSS_STATUS_ XX) Mnemonic, Bit |
|---|---|---|---|---|
| 47, 0 | PSM-44 | ±15 Supplies to TEU A-side OFF | E00D - C00D | _01, 3 = 0 AND _01, 4 = 0 AND _01, 5 = 0 AND _01, 6 = 0 |
| 47, 1 | PSM-45 | ±15 Supplies to TEU A-side ON (prim) | C00D - E011 - C011 - F00D | _01, 3 = 0 AND _01, 4 = 1 AND _01, 5 = 1 AND _01, 6 = 1 |
| 47, 2 | PSM-46 | ±15 Supplies to TEU A-side ON (redt) | E00D - E011 - C011 - D00D | _01, 3 = 1 AND _01, 4 = 0 AND _01, 5 = 1 AND _01, 6 = 1 |
| 48, 0 | PSM-47 | +5 Supplies to TEU B-side OFF | E010 - C010 | _04, 1 = 0 AND _04, 0 = 0 AND _04, 2 = 0 |
| 48, 1 | PSM-48 | +5 Supplies to TEU B-side ON (prim) | C010 - E00C - C00C - C00D - E00D - F010 | _04, 1 = 1 AND _04, 2 = 1 |
| 48, 2 | PSM-49 | +5 Supplies to TEU B-side ON (redt) | E010 - E00C - C00C - C00D - E00D - D010 | _04, 0 = 1 AND _04, 2 = 1 |
| 49, 0 | PSM-50 | ±15 Supplies to TEU B-side OFF | E011 - C011 | _04, 3 = 0 AND _04, 4 = 0 AND _04, 5 = 0 AND _04, 6 = 0 |
| 49, 1 | PSM-51 | ±15 Supplies to TEU B-side ON (prim) | C011 - E00D - C00D - C00C - E00C - F011 | _04, 3 = 0 AND _04, 4 = 1 AND _04, 5 = 1 AND _04, 6 = 1 |
| 49, 2 | PSM-52 | ±15 Supplies to TEU B-side ON (redt) | E011 - E00D - C00D - C00C - E00C - D011 | _04, 3 = 1 AND _04, 4 = 0 AND _04, 5 = 1 AND _04, 6 = 1 |
| 50, 0 | PSM-53 | +5/±15 Supplies to EEA OFF | E009 - C009 - E008 - C008 | _05, 0 = 0 AND _05, 1 = 0 AND _05, 2 = 0 AND _05, 3 = 0 AND _05, 4 = 0 AND _05, 5 = 0 AND _05, 6 = 0 |
| 50, 1 | PSM-54 | +5/±15 Supplies to EEA ON (5 prim, 15 prim) | C008 - C009 - F008 - F009 | _05, 0 = 0 AND _05, 1 = 1 AND _05, 2 = 1 AND _05, 3 = 0 AND _05, 4 = 1 AND _05, 5 = 1 AND _05, 6 = 1 |
| 50, 2 | PSM-55 | +5/±15 Supplies to EEA ON (5 prim, 15 redt) | C008 - E009 - F008 - D009 | _05, 0 = 0 AND _05, 1 = 1 AND _05, 2 = 1 AND _05, 3 = 1 AND _05, 4 = 0 AND _05, 5 = 1 AND _05, 6 = 1 |
| 50, 3 | PSM-56 | +5/±15 Supplies to EEA ON (5 redt, 15 prim) | E008 - C009 - D008 - F009 | _05, 0 = 1 AND _05, 1 = 0 AND _05, 2 = 1 AND _05, 3 = 0 AND _05, 4 = 1 AND _05, 5 = 1 AND _05, 6 = 1 |
| 50, 4 | PSM-57 | +5/±15 Supplies to EEA ON (5 redt, 15 redt) | E008 - E009 - D008 - D009 | _05, 0 = 1 AND _05, 1 = 0 AND _05, 2 = 1 AND _05, 3 = 1 AND _05, 4 = 0 AND _05, 5 = 1 AND _05, 6 = 1 |

Note 1. This IRC requires not less than 100ms interval before next IRC is sent.

### 3.4 Mechanical Interface

N/A

### 3.5 Thermal Interface

N/A

### 3.6 Optical Interface

N/A

### 3.7 Other Interfaces

N/A

# 4 ABBREVIATIONS & ACRONYMS

| | |
|---|---|
| ADC | Analog to Digital Converter |
| C&TH | Command and Telemetry Handbook |
| ICD | Interface Control Document |
| IFC | In-Flight Calibrator (Subsystem) |
| IICD | Internal Interface Control Document |
| IPS | Instrument Processor Subsystem |
| IPU | Instrument Processor Unit |
| ITS | Instrument Technical Specification |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| PCU | Power Converter Unit |
| SPU | Signal Processing Unit |
| TBD | To Be Determined |
| TBV | To Be Verified |
| TSS | Telescope Subsystem |