HIRDLS

TT-OXF-232

HIGH RESOLUTION DYNAMICS LIMB SOUNDER

Originator:

Date: 18 Nov 99

Subject/Title: **IFC BEU circuit board thermal analysis**

Description/Summary/Contents:

Board & component level thermal analysis for the electronic circuits housed in the IFC electrical unit (BEU)

Report prepared by Rutherford Appleton Laboratory.

Keywords: GMU, circuit, thermal, analysis

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CLRC RUTHERFORD APPLETON LABORATORY	HIRDLS / IFC-BEU Thermal Analysis	Doc.No: RAL-HIR-BEU-TN-001 Issue : 3 Date : 11 November 1999 Page : 1

TECHNICAL NOTE

HIRDLS / IFC-BEU Thermal Analysis

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CONTENTS

1 Scope

To determine the EOL, worst-case, hot temperatures of some critical devices on the circuit boards within the black body electronics box of the HIRDLS in-flight calibrator subsystem.

This information will also then be used by by the Atmospheric, Oceanic and Planetary Physics (AOPP) group at Oxford University to calculate the junction temperatures of the critical components, and hence to verify the thermal design of the box.

The following data has been supplied to RAL by the AOPP group:

- BEU box engineering drawing
- Thermal interface description
- Cabling details
- Description of BEU & circuit board assembly and heat sink concept.
- Component packaging data (FETs and ICs)
- Power dissipations for logic, analogue and auxiliary PCBs
- Layout and component dissipations for auxiliary PCBs.

2 Applicable Documents

2.1 Thermal interface requirements document SP-HIR-111, L Osborne
Lockheed Martin Missiles & Space (LMMS), 23rd April 1999

2.2 Design of the 118 mK kapton heat sink and heat flow calculations for wiring harness
Atmospheric, Oceanic and Planetary Physics (AOPP), Oxford University

3 Thermal Design

3.1 Internal Design Features

Box Panels
The panels of the box are typically 1 mm thick and their respective dimensions are 80.0 x 172.0 x 240.0 mm. The panels are held together using M2 screws (8 for +X/+Y and +Z/+X interface, 3 for +Y/+Z interface). A bare metal interface through a 1 mm thick plate has been assumed for each M2 screw, producing a conductance of 0.090 W/K.

Printed Circuit Boards Mounting Method
Prime and redundant sides of the box each contain three PCBs:
- Analogue PCB
- Logic PCB
- Auxiliary PCB

Each PCB is mounted using 14 small aluminium blocks around the perimeter. Each block is screwed to both the PCB and the box walls using M1.6 screws. An M1.6 interface produces a conductance of 0.080 W/K.

Heat Sinks
No method of heat sinking has been taken into account in this analysis, but this may be required (by supplying a heat strap between the transistors and outer walls), depending on the functional limitations and reliability requirements.

3.2 External Design Features

Attachment to the +X side of the BEU to STH

The BEU is hard mounted to the +X side of the panel which separates the EU cavity from the OBA cavity. Six bolts of M4 type attach the box to this platform, with a total foot area of 340 mm2.

4 Geometric Mathematical Model

4.1 Geometry

A geometric mathematical model of the BEU box has been created using ESARAD software. The model includes all external and internal walls of the BEU box, plus:

- PCBs, FETs and ICs
- Cylinders within the box

External surfaces of the box are modelled as inactive, as the thermal environment has been defined for each external surface by LMMS.
The dimensions used for the components in the BEU geometric mathematical model are described in Table 4.1, below. The electronics box GMM is shown in Figure 4.1.

Items	Location	Dimensions (mm)
PCB1 Analogue (primary)	unit	68.0 x 228.0
PCB1 Logic (primary)	unit	68.0 x 228.0
PCB1 Auxiliary (primary)	unit	68.0 x 228.0
PCB2 Analogue (redundant)	unit	68.0 x 228.0
PCB2 Logic (redundant)	unit	68.0 x 228.0
PCB2 Auxiliary (redundant)	unit	68.0 x 228.0
TO99_U7_ON	PCB1 Auxiliary	Ø = 8 ; h = 4.5
TO99_U8_ON	PCB1 Auxiliary	Ø = 8 ; h = 4.5
TO99_U9_ON	PCB1 Auxiliary	Ø = 8 ; h = 4.5
ICs_U11_ON	PCB1 Auxiliary	2.92 x 7.24 x 11.2
ICs_U16_ON	PCB1 Auxiliary	2.92 x 7.24 x 11.2
TO99_U7_OFF	PCB2 Auxiliary	Ø = 8 ; h = 4.5
TO99_U8_OFF	PCB2 Auxiliary	Ø = 8 ; h = 4.5
TO99_U9_OFF	PCB2 Auxiliary	Ø = 8 ; h = 4.5
ICs_U11_OFF	PCB2 Auxiliary	2.92 x 7.24 x 11.2
ICs_U16_OFF	PCB2 Auxiliary	2.92 x 7.24 x 11.2

Table 4.1 - PCBs geometric features

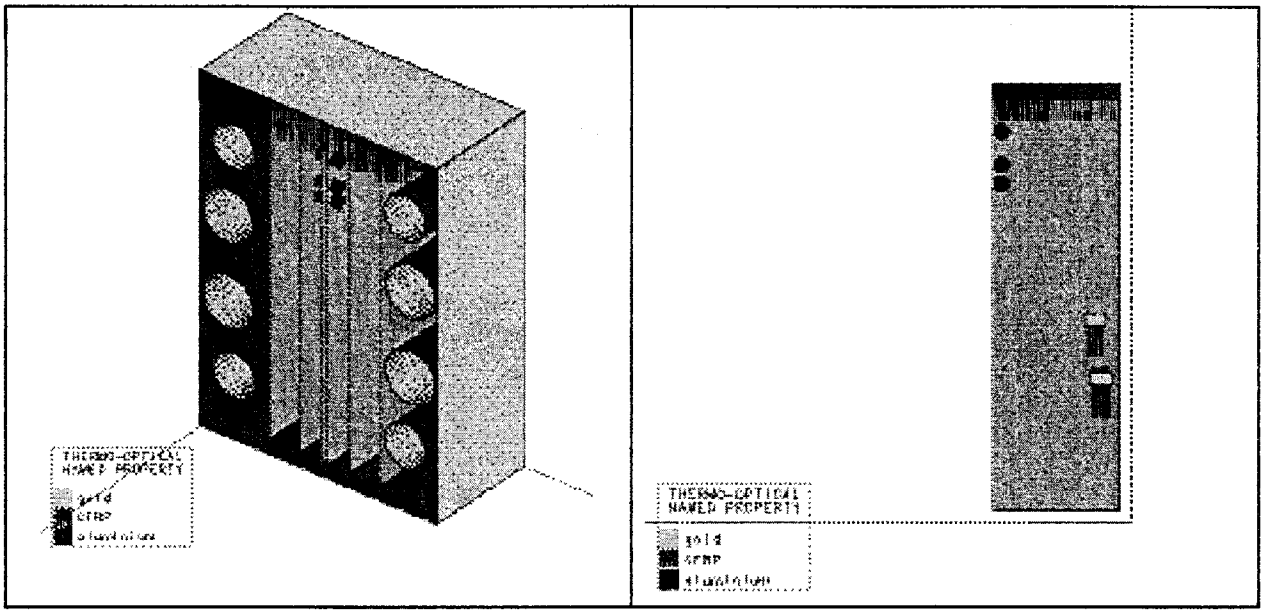

Figure 4.1 - BEU Geometric Mathematical Model

4.2 Thermo-Optical Properties

EOL properties for Polished Gold surfaces were given by LMMS. Other properties are described in Table 4.2.

Material	α_s		ε_{IR}	
	EOL	BOL	EOL	BOL
Polished GOLD	0.30	0.30	0.05	0.05
GFRP	0.72	0.72	0.89	0.89
Aluminium 6068	0.14	0.14	0.09	0.09

Table 4.2 - Thermal-Optical Properties

5 Thermal Environment

5.1 Environmental Loads

There are no solar, albedo or earthshine loads on the BEU, as it is housed inside the spacecraft.

5.2 External Radiative Couplings

Radiative couplings and sink temperatures for the external BEU walls are shown below, as defined in AD2.1.

		BOL Operation	EOL Operation
	Radiative link to Sink T (e x F x Area), cm2	Sink T °C	Sink T °C
+X surface	19.6	-10.8	23.3
-X surface	20.2	-6.9	26.6
+Y surface	11.9	-8.8	25.0
-Y surface	12.8	-9.9	24.4
+Z surface	8.8	-11.2	22.8
-Z surface	9.0	-8.0	26.2

Table 5.2 – Radiative Environment

5.3 Conductive Interface temperature

The STH steady state temperature at the interface is defined in AD 2.1 as 1 as being between –8.3 °C and 25.8 °C during normal operation.

IFC-BB and IPU are boundary nodes and their operational predicted maximum temperatures are assumed to be respectively 43°C and 36°C (These values are drawn from the last HIRDLS CDR, held at RAL during September 1999).

6 Thermal Model

6.1 Nodal Discretisation

The model consists of 30 diffuse nodes and 9 boundary nodes representing the spacecraft (1 node), the cavity mezzanine (6 nodes) where the BEU box is mounted, the IFC-BB (1 node) and IPU (1 node) units. A full node listing is given in **Table 6.1** describing the nodal distribution as well as locations and surface properties of each node.

Node Number	Node Type	Items	Surface
10	D	BEU –X	Polished Gold (out) / Aluminium (in)
20	D	BEU +X	Polished Gold (out) / Aluminium (in)
30	D	BEU –Y	Polished Gold (out) / Aluminium (in)
40	D	BEU +Y	Polished Gold (out) / Aluminium (in)
50	D	BEU –Z	Polished Gold (out) / Aluminium (in)
60	D	BEU +Z	Polished Gold (out) / Aluminium (in)
100	D	PCB1 Analogue (primary)	GFRP
110	D	PCB1 Logic (primary)	GFRP
120	D	PCB1 Auxiliary (primary)	GFRP
200	D	PCB2 Analogue (redundant)	GFRP
210	D	PCB2 Logic (redundant)	GFRP
220	D	PCB2 Auxiliary (redundant)	GFRP
107	D	TO99_U7_ON	Aluminium
108	D	TO99_U8_ON	Aluminium
109	D	TO99_U9_ON	Aluminium
111	D	ICs_U11_ON	Polished Gold
116	D	ICs_U16_ON	Polished Gold

207	D	TO99_U7_OFF	Aluminium
208	D	TO99_U8_OFF	Aluminium
209	D	TO99_U9_OFF	Aluminium
211	D	ICs_U11_OFF	Polished Gold
216	D	ICs_U16_OFF	Polished Gold
300	D	Cylinder	Aluminium
310	D	Cylinder	Aluminium
320	D	Cylinder	Aluminium
330	D	Cylinder	Aluminium
340	D	Cylinder	Aluminium
350	D	Cylinder	Aluminium
360	D	Cylinder	Aluminium
370	D	Cylinder	Aluminium
1000	B	-X Surface Sink T	-
1500	B	STH	-
2000	B	+X Surface Sink T	-
3000	B	-Y Surface Sink T	-
4000	B	+Y Surface Sink T	-
5000	B	-Z Surface Sink T	-
6000	B	+Z Surface Sink T	-
10000	B	IFC-BB	-
20000	B	IPU	-

Table 6.1 - Node listing

6.2 Conductive Couplings

Printed Circuit Boards:
The PCBs are modelled as individual thermal nodes. All the components (FETs and ICs) mounted onto the auxiliary PCBs have been modelled individually as well.

The PCBs are manufactured from standard 1.6 mm thick GFRP (with four 75μm thick copper planes). It is assumed that approximately half of the copper has been removed. Therefore an effective conductivity for the PCBs has been calculated, considering the PCB plane as a combination of a copper layer (thickness = 0.15mm) and a GFRP layer (thickness = 1.45mm). This produces an effective thermal conductivity 36.32 W/m/K.

Regarding FETs and ICs, the base metal of pins is assumed to be copper whose thermal conductivity equals to 385 W/m/K.

Harnesses:
Two harnesses connect up the box at +Z/-Z level to the IFC-BB component and to the IPU. Conductances due to both harnesses have been assessed while referring to ref. 2.

- to IFC-BB (in-flight calibrator black body)

This harness consists of 32 microcoaxials, 8x26AWG and 384x36AWG in parallel (L=1.50m). The harness conductance is calculated to be 0.00283W/K.

- to IPU

This harness consists of 38x26AWG and 4 small inner shields (72x36AWG) in parallel (L=1.50m). The harness conductance is calculated to be 0.00229W/K.

Table 6.2 below gives the calculated conductances between the various nodes.

Node Number	Node Number	Coupling Type	Conductance (W/K)
20	60	8×M2	0.1552
60	10	8×M2	0.1552
10	50	8×M2	0.1552
50	20	8×M2	0.1552
20	30	8×M2	0.1526
30	10	8×M2	0.1526
10	40	8×M2	0.1526
40	20	8×M2	0.1526
60	40	3×M2	0.0650
40	50	3×M2	0.0650
50	30	3×M2	0.0650
30	60	3×M2	0.0650
10	1500	6×M4	1.4171
100	10	7×M1.6	0.1420
100	20	5×M1.6	0.1180
100	50	1×M1.6	0.0177
100	60	1×M1.6	0.0177
110	10	7×M1.6	0.1528
110	20	5×M1.6	0.1254
110	50	1×M1.6	0.0182
110	60	1×M1.6	0.0182
120	10	7×M1.6	0.1617
120	20	5×M1.6	0.1314
120	50	1×M1.6	0.0185
120	60	1×M1.6	0.0185
107	120	Soldered	0.0663
108	120	Soldered	0.0663
109	120	Soldered	0.0663
111	120	Soldered	0.0047
116	120	Soldered	0.0749
50	10000	Harness	0.00283
60	20000	Harness	0.00229

Table 6.2 - Conductive couplings

7 Power Dissipation

Item	Number of components	Number of components on simultaneously	Dissipation (W)	Max case temperature (°C)	Max junction temperature (°C)
PCBs Analogue	2	1	1.305	TBD	TBD
PCBs Logic	2	1	0.110	TBD	TBD
PCBs Auxiliary	2	1	0.130	TBD	TBD
TO99_U7	2	1	0.080	TBD	TBD
TO99_U8	2	1	0.080	TBD	TBD
TO99_U9	2	1	0.110	TBD	TBD
ICs_U11	2	1	0.075	TBD	TBD
ICs_U16	2	1	0.150	TBD	TBD

Table 7.1 – EOL BEU Power Dissipation

1. the Analogue PCB dissipates (max) 1305 mW, assumed to be evenly distributed over the board
2. the Logic PCB dissipates 110 mW (evenly distributed)

3. the Auxiliary PCB dissipates a total of 625 mW, of which:
   - 80 mW is dissipated in two of the output FETs
   - 110 mW in the third
   - 150 mW in a 16-pin flat pack microcircuit (not mentioned at our meeting)
   - 75 mW in a second 1-pin flat pack microcircuit.
   - the remainder evenly distributed

Total power dissipated in the box is therefore 2.04 W.

8 Steady State Analysis Results

8.1 BOL steady-state operational case

Predicted temperature for each side of the box, primary components and redundant components are given in the following Table 8.1.

NODE	LABEL	T (°C)	QI (W)
10	BEU_MX	-8.27	0.00
20	BEU_PX	-8.26	0.00
30	BEU_MY	-8.26	0.00
40	BEU_PY	-8.25	0.00
50	BEU_MZ	-8.16	0.00
60	BEU_PZ	-8.23	0.00
100	PCB1 Analogue	-8.25	0.00
107	TO99_U7_ON	-8.25	0.00
108	TO99_U8_ON	-8.25	0.00
109	TO99_U9_ON	-8.25	0.00
110	PCB1 Logic	-8.25	0.00
111	ICs_U11_ON	-8.25	0.00
116	ICs_U16_ON	-8.25	0.00
120	PCB1 Auxiliary	-8.25	0.00
200	PCB2 Analogue	-8.25	0.00
207	TO99_U7_OFF	-8.25	0.00
208	TO99_U8_OFF	-8.25	0.00
209	TO99_U9_OFF	-8.25	0.00
210	PCB2 Logic	-8.25	0.00
211	ICs_U11_OFF	-8.25	0.00
216	ICs_U16_OFF	-8.25	0.00
220	PCB2 Auxiliary	-8.25	0.00
300	CYLINDER11	-8.25	0.00
310	CYLINDER12	-8.25	0.00
320	CYLINDER13	-8.26	0.00
330	CYLINDER14	-8.25	0.00
340	CYLINDER21	-8.25	0.00
350	CYLINDER22	-8.25	0.00
360	CYLINDER23	-8.25	0.00
370	CYLINDER24	-8.25	0.00
1000	MX Sink T	-6.90	0.00
1500	STH	-8.30	0.00
2000	PX Sink T	-10.80	0.00
3000	MY Sink T	-9.90	0.00
4000	PY Sink T	-8.80	0.00
5000	MZ Sink T	-8.00	0.00
6000	PZ Sink T	-11.20	0.00
10000	IFC-BB	11.00	0.00
20000	IPU	4.00	0.00

Table 8.1 - Predicted Node Temperatures - Steady State Case - BOL Operational

8.2 EOL steady-state operational case

Predicted temperature for each side of the box, primary components and redundant components are given in the following Table 8.1.

NODE	LABEL	T (°C)	QI (W)
10	BEU_MX	27.17	0.00
20	BEU_PX	28.35	0.00
30	BEU_MY	27.82	0.00
40	BEU_PY	27.79	0.00
50	BEU_MZ	28.03	0.00
60	BEU_PZ	27.97	0.00
100	PCB1 Analogue	31.29	1.30
107	TO99_U7_ON	30.44	0.08
108	TO99_U8_ON	30.44	0.08
109	TO99_U9_ON	30.89	0.11
110	PCB1 Logic	28.71	0.11
111	ICs_U11_ON	44.17	0.07
116	ICs_U16_ON	31.23	0.15
120	PCB1 Auxiliary	29.24	0.13
200	PCB2 Analogue	27.77	0.00
207	TO99_U7_OFF	27.99	0.00
208	TO99_U8_OFF	27.99	0.00
209	TO99_U9_OFF	27.99	0.00
210	PCB2 Logic	27.80	0.00
211	ICs_U11_OFF	27.98	0.00
216	ICs_U16_OFF	27.99	0.00
220	PCB2 Auxiliary	27.99	0.00
300	CYLINDER11	30.28	0.00
310	CYLINDER12	30.34	0.00
320	CYLINDER13	30.35	0.00
330	CYLINDER14	30.29	0.00
340	CYLINDER21	27.82	0.00
350	CYLINDER22	27.80	0.00
360	CYLINDER23	27.80	0.00
370	CYLINDER24	27.81	0.00
1000	MX Sink T	26.60	0.00
1500	STH	25.80	0.00
2000	PX Sink T	23.30	0.00
3000	MY Sink T	24.40	0.00
4000	PY Sink T	25.00	0.00
5000	MZ Sink T	26.20	0.00
6000	PZ Sink T	22.80	0.00
10000	IFC-BB	43.00	0.00
20000	IPU	36.00	0.00

Table 8.2 - Predicted Node Temperatures - Steady State Case - EOL Operational

9 Sensitivity Analysis

Owing to:

1. a reduction of the PCB conductivity from 36.32 W/(m/K) to 18.29 W/(m/K), considering the PCB plane as a combination of two copper planes (instead of four as initially assumed, i.e. an equivalent copper plane 0.075 mm thick, instead of 0.15 mm) and a GFRP layer (with thickness therefore equals to 1.525mm).

2. a reduction of the bolted joints conductivity as follows,

   - an M2 conductance of 0.075 W/k (instead of 0.090 W/k as initially assumed)
   - an M1.6 conductance of 0.06 W/K (instead of 0.080 W/k as initially assumed)

the IFC-BEU thermal model has been re-run to check its sensitivity to the aforementioned parameters.

		Predicted Temperature Previous thermal model	Predicted Temperature Updated thermal model	Power Dissipation
NODE	LABEL	T (°C)	T (°C)	Q (W)
10	BEU_MX	27.17	27.16	0.00
20	BEU_PX	28.35	28.70	0.00
30	BEU_MY	27.82	28.03	0.00
40	BEU_PY	27.79	27.96	0.00
50	BEU_MZ	28.03	28.23	0.00
60	BEU_PZ	27.97	28.16	0.00
100	PCB1 Analogue	31.29	32.88	1.30
107	TO99_U7_ON	30.44	31.33	0.08
108	TO99_U8_ON	30.44	31.33	0.08
109	TO99_U9_ON	30.89	31.78	0.11
110	PCB1 Logic	28.71	29.62	0.11
111	ICs_U11_ON	44.17	45.05	0.07
116	ICs_U16_ON	31.23	32.11	0.15
120	PCB1 Auxiliary	29.24	30.12	0.13
200	PCB2 Analogue	27.77	27.98	0.00
207	TO99_U7_OFF	27.99	28.42	0.00
208	TO99_U8_OFF	27.99	28.42	0.00
209	TO99_U9_OFF	27.99	28.42	0.00
210	PCB2 Logic	27.80	28.07	0.00
211	ICs_U11_OFF	27.98	28.41	0.00
216	ICs_U16_OFF	27.99	28.42	0.00
220	PCB2 Auxiliary	27.99	28.42	0.00
300	CYLINDER11	30.28	31.51	0.00
310	CYLINDER12	30.34	31.58	0.00
320	CYLINDER13	30.35	31.59	0.00
330	CYLINDER14	30.29	31.51	0.00
340	CYLINDER21	27.82	28.04	0.00
350	CYLINDER22	27.80	28.02	0.00

360	CYLINDER23	27.80	28.01	0.00
370	CYLINDER24	27.81	28.03	0.00
1000	MX Sink T	26.60	26.60	0.00
1500	STH	25.80	25.80	0.00
2000	PX Sink T	23.30	23.30	0.00
3000	MY Sink T	24.40	24.40	0.00
4000	PY Sink T	25.00	25.00	0.00
5000	MZ Sink T	26.20	26.20	0.00
6000	PZ Sink T	22.80	22.80	0.00
10000	IFC-BB	43.00	43.00	0.00
20000	IPU	36.00	36.00	0.00

Table 9.1 - Predicted Node Temperatures - Steady State Case - EOL Operational

Conclusion:

It turns out that the impact on temperatures is fairly insignificant, since the auxiliary PCB and highest predicted temperature increase (occurring at IC U11, node 111), due to reduction in PCB and bolted joints conductivity, is less than 0.9°C.

However, the analogue PCB (node 100), which dissipates 1.3 W, reaches a temperature almost 1.6° higher compared to the previous thermal model.

10 Thermal Balance

Amounts of heat that are radiatively or conductively rejected out from each side of the box have been estimated to check out if the sum of these values is consistent with the thermal dissipation (equals to 2.04 W) assumed for the box during EOL operation.

- Radiative heat transfer from box to cavity

Node at temperature Ti	Node at temperature To	Gr , Radiative coupling to sink temperature To (m2)	Ti (°C)	To (°C)	Ti (K)	To (K)	Qr (W)
20	2000	0.00196	28.70	23.30	301.85	296.45	0.06
10	1000	0.00202	27.16	26.60	300.31	299.75	0.01
40	4000	0.00119	27.96	25.00	301.11	298.15	0.02
30	3000	0.00128	28.03	24.40	301.18	297.55	0.03
60	6000	0.00088	28.16	22.80	301.31	295.95	0.03
50	5000	0.00090	28.23	26.20	301.38	299.35	0.01
							Qr,tot = 0.16

- Conductive heat transfer from box to shelf (STH)

Node at temperature Ti	Node at temperature To	Gc, Conductive coupling to shelf at temperature To (W/K)	Ti (°C)	To (°C)	Qc (W)
10	1500	1.4171	27.16	25.80	1.93
					Qc,tot = 1.93

Table 10.1 - Overall Thermal Balance

NB:

Qr = Gr.σ [illegible], σ = 5.67.10e-8 [illegible]

Qc = Gc.(Ti -To)

Conclusion :

The total amount of heat worked out is 2.09 W and barring approximation errors, is consistent with assumptions of thermal dissipation of the box.

92.3 % of this total amount of heat is conductively rejected out through the shelf (STH) on which the IFC-BB box is mounted.

11 Summary

The highest power components in the BEU are mounted to the power converter board. This board was modelled as a single node, with the individual components modelled as additional nodes conductively coupled to the board. The resulting temperatures are therefore conservative, as they assume that all the heat is dumped into the centre of the board. More detailed modelling of a discretised PCB does not appear necessary, as the resulting temperature predictions were relatively low.
Analysis results show that the highest predicted temperature within the BEU box occurs at IC U11 (node 111), which reaches 44°C at EOL.
The transistor power dissipations are relatively low, and their maximum predicted case temperature are all below 31°C. As a result, it does not appear to be necessary to incorporate a heat sink onto these components.