HIRDLS

HIGH RESOLUTION DYNAMICS LIMB SOUNDER

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IFC to IPS Interface Control Document (ICD)

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Log of Changes

Rev.	Date	Section	Change Description	Approved by:
Initial Release	98-06-22			
Rev. A	99-11-10	3.2	Fig. 3.2-2: a. Deleted +28REG_PWR/RTN lines (TCP-042R1) b. added BEU-side link between 5_RTN and 15_RTN c. added IPU-side circuit for AD590s d. removed inner-shield ground connections on BEU side	
		3.2.1.2	Reworded to correspond to changes in Fig. 3.2-2.	
		3.2.2	Table 3.2.2-1: deleted +28 V Reg. column; updated +15 V currents (TCP-042R1).	
		3.2.3.6	Paragraph a): revised per Hepplewhite input	
		3.2.5.2	Table 3.2.5.2-1: deleted +28REG_PWR and +28REG_RTN lines (TCP-042R1); raised Imax to 200 mA on +15_PWR and 15_RTN lines to be consistent with new current values in Table 3.2.2-1.	
		3.3	Deleted obsolete reference to TC-UCB-009.	
		4	Added several missing acronyms.	
Rev. B	00-07-21	2.1	Provided revision dates for referenced documents	
		3.2	Figure 3.2-2. Replaced wire links between A_IFC_5_RTN and A_IFC_15_RTN on BEU end of cable with 1K resister and replaced wire links between B_IFC_5_RTN and B_IFC_15_RTN on BEU end of cable with 1K resister.	
Rev C	00-10-20	3.2.1.2	Add text " through 1 KΩ resistor"	
	00-10-30	3.2	Figure 3.2-2. Modify IPU side of interface depiction of IFC AD590 interface to show MUX'd +10V drive. (CR184)	
		3.2.5.2	Table 3.2.5.2-1 Swap BEU pin #s 1 and 19 for IFC_BBFPT2_DRV and IFC_BBFPT2_SEN. To compensate for an error in the BEU (CR181)	
Rev D	00-11-20	3.3	Modified entire section to accommodate C&TH requirements. (CR189)	
		4.0	Added HCW and DRW to list of acronyms (CR189)	
	01-04-18	3.3.1.1	Added Table 3.3.1.1-2 from C&TH Vol1 2.6.3.2.2-2 based on RE comments. (CR189)	
Rev E	01-07-30	3.2.2	Table 3.2.2-1. Change the voltage limits: 1) to be measured at the IFC end of the cable and 2) reduce voltage levels. (CR216)	R. von Savoye J. Whitney C. Hepplewhite R. Lindgren A. McField /s/

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1 SCOPE

Interface Control Documents (ICDs) in the SP-HIR-2XX series define, as applicable, the specific design implementations of the Electrical, Functional, Mechanical, Thermal Conductive, and Optical interfaces between specified HIRDLS Subsystems.

This ICD defines the interface between the In-Flight Calibration Subsystem (IFC) and the Instrument Processor Subsystem (IPS). This interface consists only of the electrical interfaces between the Black-body Electronics Unit (BEU) and Instrument Processor Unit (IPU).

For the interface between the BEU and the IFC Black Body (IBB), refer to SP-HIR-266.

2 DOCUMENT REFERENCES

2.1 Applicable Documents

The documents listed below are a part of this ICD to the extent specified herein. In the case of a conflict between the contents of this ICD and any Applicable Document, this ICD shall take precedence.

GSFC 424-28-21-13	Instrument Technical Specification (ITS)	00-02
SP-HIR-200G	IICD System Section	97-12-01
ANSI/TIA/EIA 422-B	Electrical Characteristics of Balanced Voltage	1994
SP-HIR-169	HIRDLS Power Distribution, Switching and Grounding	00-02-01

2.2 Information Documents

The documents listed below are explicitly not, by reference, part of this ICD, but contain information that may be relevant to the interpretation and understanding of this ICD.

SP-HIR-216	STH to IFC Interface Control Document (ICD)	Current Revision
SP-HIR-246	TSS to IFC Interface Control Document (ICD)	Current Revision
SP-HIR-266	IFC Black Body to Black Body Electronics Unit Interface Control Document	Current Revision

3 INTERFACE REQUIREMENTS

3.1 Interface Concept Overview

The interface between the IPU and the BEU consists of separate A-side and B-side electrical interfaces for power and for control and data signals. Control and Data transfers in either direction take place over dedicated unidirectional differential serial circuits. Transfers in either direction are synchronous, with the clock signal being provided by the IPU. IFC Power is supplied from the IPU. There are no mechanical, thermal, or optical interfaces between these subsystems.

A conceptual block diagram of these interfaces is shown in Figure 3.1-1.

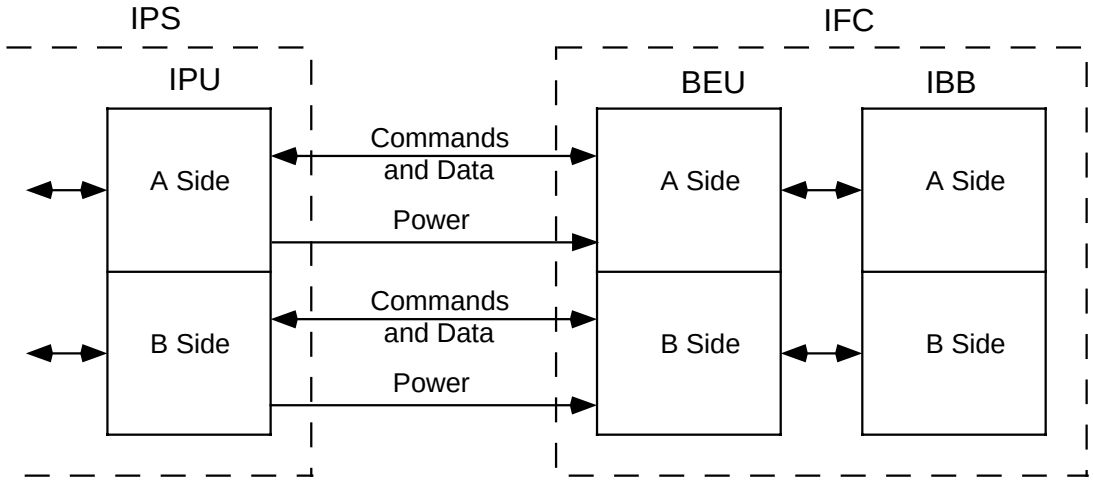

Figure 3.1-1 IPS-IFC Interfaces

3.2 Electrical Interface

Power and Data interfaces between the IPU and the BEU are implemented via a single cable assembly, the configuration of which is shown in Figure 3.2-1.

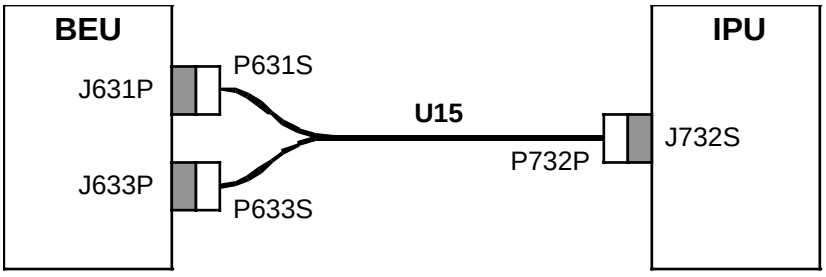

Figure 3.2-1 IPS-IFC Cable/Connector Identification

Figure 3.2-2 shows the signal names of the Power and Control/Data interfaces, with the shielding configuration and, where relevant, the sending/receiving devices.

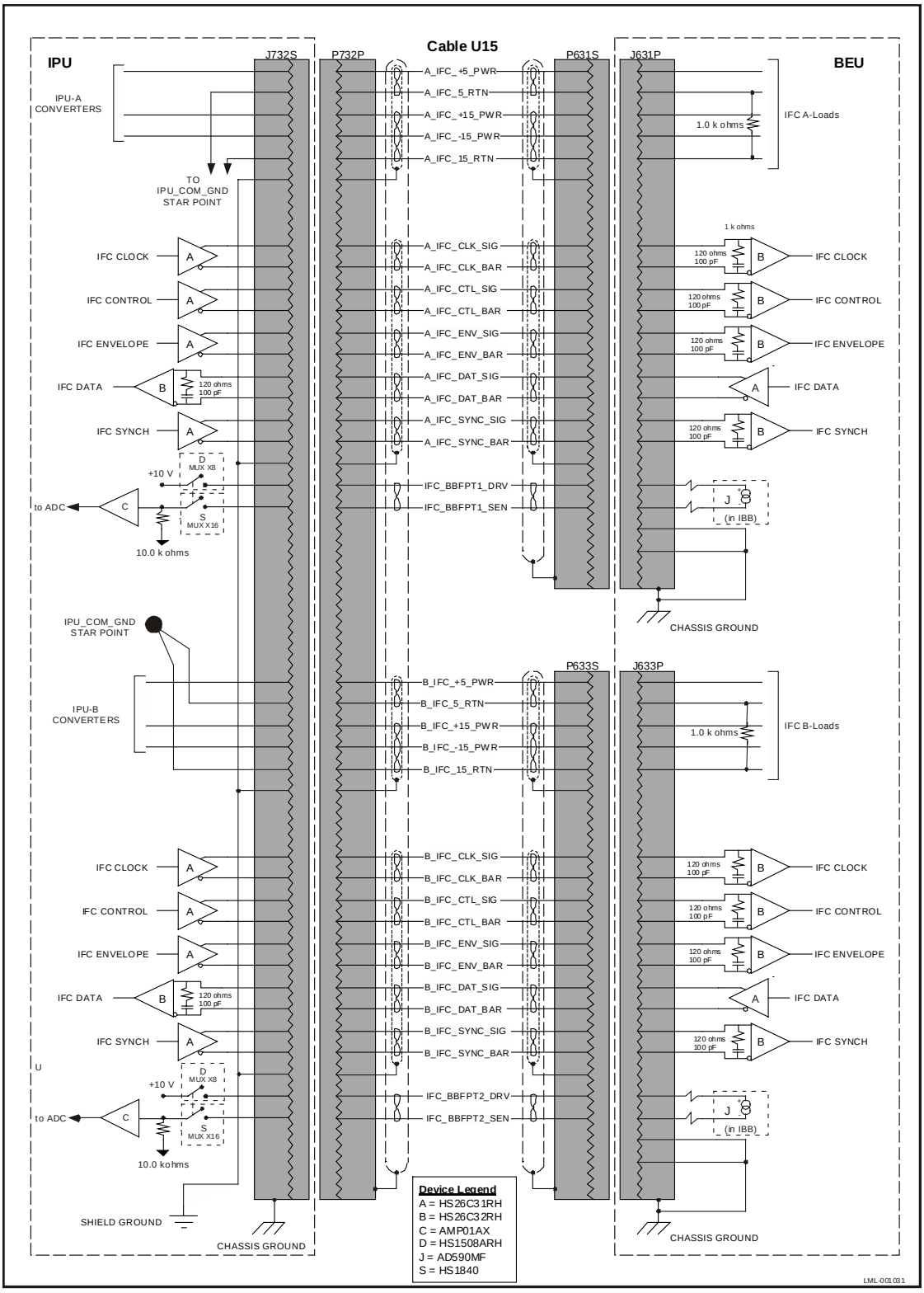

Figure 3.2-2 IPU-BEU Power, Control, and Data Interconnection

3.2.1 Grounding and Shielding

3.2.1.1 Primary Power Grounding and Shielding

N/A

3.2.1.2 Secondary Power Grounding and Isolation

On the BEU side of this interface, the 5_RTN, 15_RTN lines shall be connected together through a 1 KΩ resistor and shall be isolated from chassis ground by > 10 MΩ and < 50 nF.

3.2.1.3 Equipment Enclosure Grounding, Shielding, and Bonding

See SP-HIR-216 and SP-HIR-246

3.2.1.4 Wire and Cable Shield Grounds

See Section 3.2.5.3

3.2.2 Power Interface

The IPU shall supply electrical power to the BEU. The supply and load characteristics are specified in Table 3.2.2-1. In this context, "DC" means for time periods longer than 5 s.

Table 3.2.2-1 Supply and Load Characteristics

	+5 V	**+15 V**	**-15 V**	**See Note**
Voltage limits at IFC end of cable (V)	+4.80 +5.10	+14.75 +15.15	-14.75 -15.15	1
Mean DC load current (mA)	60	136	60	2
Maximum DC load current (mA)	60	170	60	3
Maximum resistance of cable + connector pins	300 mΩ	300 mΩ	300 mΩ	
Maximum supply output resistance	100 mΩ (DC to 5 kHz)	100 mΩ (DC to 5 kHz)	100 mΩ (DC to 5 kHz)	4
Converter-induced spikes at IPU end of cable	<150 mV peak at ~25 MHz	<150 mV peak at ~25 MHz	<150 mV peak at ~25 MHz	5
IPU-induced ripple at IPU end of cable, 0-5 MHz	<250 mV peak	<250 mV peak	<250 mV peak	
IPU-induced ripple at IPU end of cable, 0-250 Hz		<100 mVp-p	<100 mVp-p	

Notes:

1. At specified mean DC load current
2. Normal steady-state operation
3. At max. BB heater setting
4. Represents load regulation at converters, i.e. 1 mV per 10 mA (max.)
5. Damped ringing on switching pulse with repetition rate of approx. 500 kHz

3.2.3 Control and Data Interface

The Control and Data interface between the IPU and BEU shall consist of redundant (A- and B-side) sets of serial control and data lines. The following descriptions, unless otherwise indicated, apply to both the A-side and the B-side.

The IPU to BEU serial Control and Data interface shall consist of five ANSI/TIA/EIA-422-B (RS-422) balanced voltage digital interface circuits. Each circuit shall be terminated in one place at the receiving end with a 120 Ω 5% resistor in series with a 100 pF 10% capacitor, connected across the inputs to the differential receiver as shown in Figure 3.2-2. Control and data transfers shall be fully synchronous and all causal signals shall be defined as active low. The differential receiver circuit shall be fail safe to an output high for a high impedance input. Active low causal signals will therefore be inactive when receiver differential inputs are disconnected. The differential driver outputs shall be defined as follows:

a. logic one: high level on the non-inverting output and a low level on the inverting output
b. logic zero: low level on the non-inverting output and a high level on the inverting output.

The differential receiver inputs shall be defined as follows:

c. logic one: high level on the non-inverting input and a low level on the inverting input.
d. logic zero: low level on the non-inverting input and a high level on the inverting input.

The five serial Control and Data interface signals are listed in Table 3.2.3-1, with the causal signals indicated.

Table 3.2.3-1 Control-Data Interface Signals

Name	Causal
IFC Clock	•
IFC Control	
IFC Envelope	•
IFC Data	
IFC Synch	

3.2.3.1 IFC Clock

The IPU shall output to the BEU an active low 20 kHz clock signal. This clock shall act as the synchronization signal for the serial control transfer from the IPU to the BEU and as the synchronization signal for the serial data transfer from the BEU to the IPU. The IFC Clock signal shall be transmitted only while data are being transferred as shown in Figure 3.2.3.5-1. This signal shall be active low (i.e. the active state shall be logic zero).

3.2.3.2 IFC Control

The IFC Control line shall be used to transfer control words to the BEU. The control line shall be a serial data line from the IPU to the BEU. The IPU shall change the control bits on the high-to-low (inactive-to-active) transition (leading edge) of the IFC Clock signal, and the BEU shall read the control bits on the low-to-high (active-to-inactive) transition (trailing edge) of the IFC Clock signal. All IFC Control words are 16 bits in length and shall be sent MSB first. Data will be transferred on the IFC Control line only while the IFC Envelope line is high (inactive) as shown in Figure 3.2.3.5-1. The IFC Control signal is high true, i.e. the high-voltage state of the receiver output is to be interpreted as a logical one.

3.2.3.3 IFC Envelope

The IFC Envelope line shall be used to define the direction in which data are to be transferred:

a. IFC Envelope inactive: control data from the IPU to the BEU

b. IFC Envelope active: status data from the BEU to the IPU

If the IFC Envelope line is high (inactive) the control data shall be transmitted synchronously with IFC Clock from the IPU to the BEU. If the IFC Envelope line is low (active), status data shall be transmitted synchronously with IFC Clock from the BEU to the IPU. The IFC Envelope line shall be valid at least one half clock cycle prior to the commencement of data transfer. The IFC Envelope signal shall be active low (i.e. the active state shall be logic zero).

3.2.3.4 IFC Data

The IFC Data line shall be used to transfer status data from the BEU to the IPU. When the IFC Envelope line is low (active), the BEU shall transmit data to the IPU. The BEU shall set data bits on the high-to-low transition (leading edge) of IFC Clock, and the IPU shall read the data bits on the low-to-high transition (trailing edge) of IFC Clock. All IFC Data words are 24 bits in length and shall be sent MSB first. The IFC Data signal shall be high true, i.e. the high-voltage state of the receiver output is to be interpreted as a logical one.

3.2.3.5 Timing

Command and Data transfer timing is shown in Figure 3.2.3.5-1.

3.2.3.6 IFC Synch

The IPU shall output to the BEU a 500 Hz synchronizing signal derived from the Chopper Reference Clock. This signal shall be phase-locked to the Chopper Reference Clock, but no particular phase offset is required. This synch signal shall be used in the BEU as follows:

a) The 500 Hz synch signal shall be divided by 4 and the resultant 125 Hz signal used to synchronize the operation of the BEU housekeeping and data acquisition sequencer.

b) The 500 Hz synch signal shall be divided by 4 and used to synchronize the operation of the AC bridge circuit at 125 Hz.

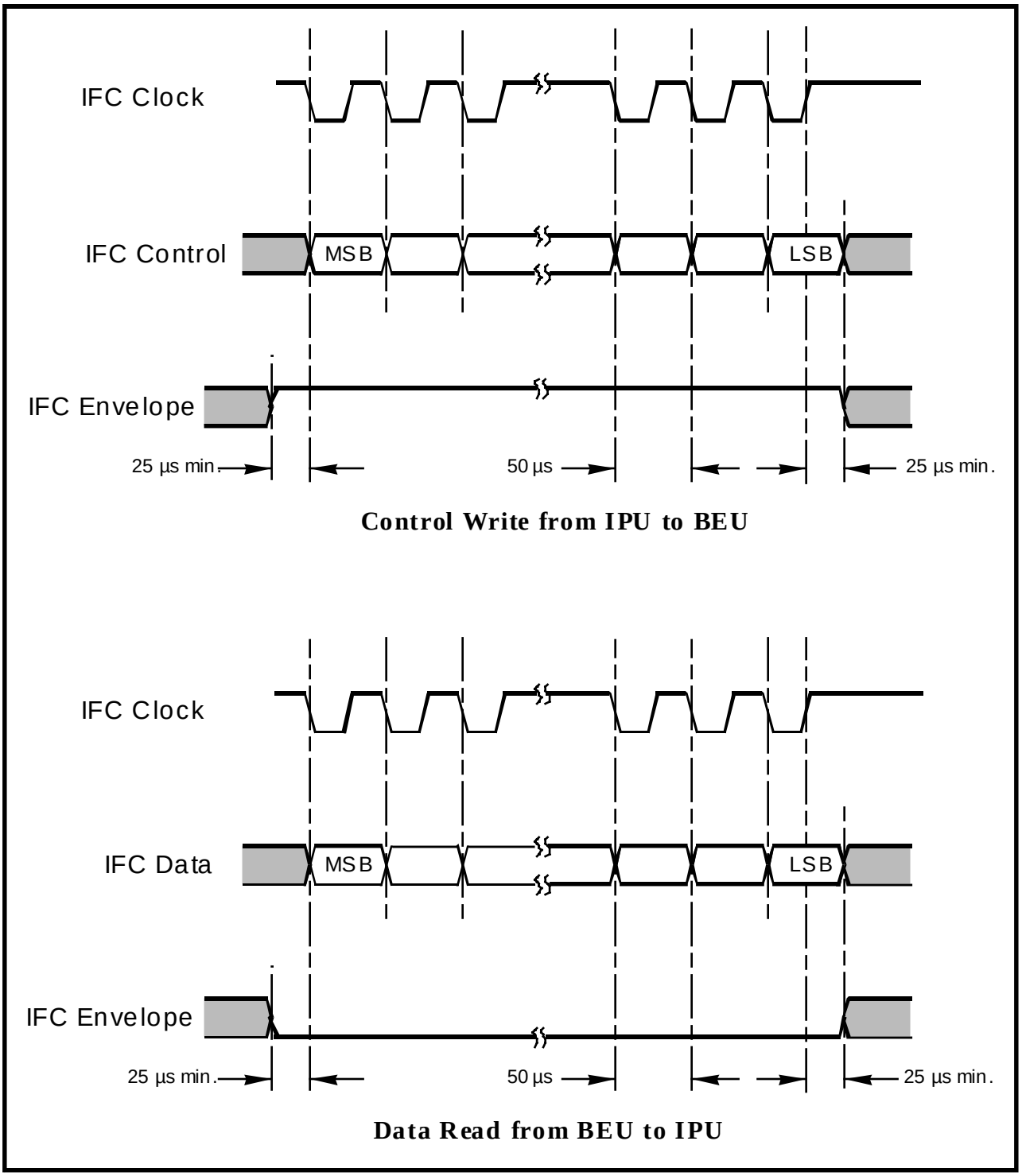

Figure 3.2.3.5-1 Control and Data Transfer Timing

3.2.4 Passive Sensor Interface

Two AD590 temperature sensors on the IBB front plate will be wired via Cable U25 to the BEU. These signals shall be passed unmodified to the IPU via Cable U15 as shown in Figure 3.2-2 and Table 3.2.5.2-1.

3.2.5 Physical Electrical Interface

3.2.5.1 Connector Definition

Connectors hard mounted on boxes or the structure are referred to as “jacks” (or receptacles) and are so indicated by a “J” prefix in the connector number. Connectors located on harnesses, cables, or wires are referred to as “plugs” and are so indicated by a “P” prefix in the connector number.

Suffix letters “P” and “S” in the connector numbers indicate, respectively, a “pin” or “socket” contact type.

Connector number assignments and the GSFC PPL-21 part numbers for the selected connector types are show in Table 3.2.5.1-1.

Table 3.2.5.1-1 Connector Types

Jack No.	Location	PPL-21 Type	Pins	Plug No.	PPL-21 Type	Cable
J732S	IPU	311P407-3S-B12	44	P732P	311P407-3P-B12	U15
J631P	BEU	311P407-2P-B12	26	P631S	311P407-2S-B12	U15
J633P	BEU	311P407-2P-B12	26	P633S	311P407-2S-B12	U15

3.2.5.2 Connector Pinout Definition

Signal names and pin assignments for Cable U15 (IPU-BEU) are defined in Table 3.2.5.2-1 (ordered by pin from the IPU side).

3.2.5.3 Wire/Cable Requirements

Unless otherwise indicated in the “WIRE TYPE” column of the pinout table, conductor sizes and insulation types shall follow accepted practice for the stated maximum voltages and currents. Other cable characteristics shall conform to military specification M27500-XX-NG-X-M-12 for shielded cable and MIL-W-81381/19-XX-X for single conductors.

Table 3.2.5.2-1 Cable U15 Pinout

Conn. No.		Location					Conn No.		
P732P		<— Cable U15 —>					P631S	P633S	
J732S		<— Box-Mounted Receptacles —>					J631P	J633P	
IPU							**A-BEU**	**B-BEU**	
Pin	**Signal Name**	**Circuit Type**	**V max** V	**I_{max}** mA	**Group**	**Wire Type**	**Pin**	**Pin**	**Function**
1	A_IFC_CLK_SIG	RS-422	6	1	T2-1A		6		CLOCK signal
2	A_IFC_CTL_SIG	RS-422	6	1	T2-2A		8		CONTROL signal
3	A_IFC_ENV_SIG	RS-422	6	1	T2-3A		25		ENVELOPE signal
4	A_IFC_DAT_SIG	RS-422	6	1	T2-4A		24		DATA signal
5	A_IFC_SYNC_SIG	RS-422	6	1	T2-5A		26		500 Hz SYNC signal
6	A_IFC_+5_PWR	PWR	6	150	T2-6A		20		+5 V power
7	A_IFC_+15_PWR	PWR	16	200	T3-1A		21		+15 V power
8	B_IFC_+15_PWR	PWR	16	200	T3-2A			2	+15 V power
9	Spare								
10	B_IFC_+5_PWR	PWR	6	150	T2-13A			2	+5 V power
11	B_IFC_CLK_SIG	RS-422	6	1	T2-8A				CLOCK signal
12	B_IFC_CTL_SIG	RS-422	6	1	T2-9A				CONTROL signal
13	B_IFC_ENV_SIG	RS-422	6	1	T2-10A			2	ENVELOPE signal
14	B_IFC_DAT_SIG	RS-422	6	1	T2-11A			2	DATA signal
15	B_IFC_SYNC_SIG	RS-422	6	1	T2-12A			2	500 Hz SYNC signal
16	A_IFC_CLK_BAR	RS-422	6	1	T2-1B		5		CLOCK complement
17	A_IFC_CTL_BAR	RS-422	6	1	T2-2B		7		CONTROL complement
18	A_IFC_ENV_BAR	RS-422	6	1	T2-3B		16		ENVELOPE complement
19	A_IFC_DAT_BAR	RS-422	6	1	T2-4B		15		DATA complement
20	A_IFC_SYNC_BAR	RS-422	6	1	T2-5B		17		500 Hz SYNC complement
21	A_IFC_5_RTN	PWR	1	150	T2-6B		2		5 V power return
22	A_IFC_15_RTN	PWR	1	200	T3-1C		12		±15 V common power return
23	A_IFC_POWER_SHD				Note 1A		14		Shield for power wire groups
24	B_IFC_15_RTN	PWR	1	200	T3-2C			1	±15 V common power return
25	B_IFC_5_RTN	PWR	1	150	T2-13B				5 V power return
26	B_IFC_CLK_BAR	RS-422	6	1	T2-8B				CLOCK complement
27	B_IFC_CTL_BAR	RS-422	6	1	T2-9B				CONTROL complement
28	B_IFC_ENV_BAR	RS-422	6	1	T2-10B			1	ENVELOPE complement
29	B_IFC_DAT_BAR	RS-422	6	1	T2-11B			1	DATA complement
30	B_IFC_SYNC_BAR	RS-422	6	1	T2-12B			1	500 Hz SYNC complement
31	Spare								
32	IFC_BBFPT1_DRV	AD590			T2-15A		1		BB Front Plate temp. sensor 1
33	IFC_BBFPT1_SEN	AD590			T2-15B		19		BB Front Plate temp. sensor 1
34	A_IFC_SIGNAL_SHD				Note 2A		23		Shield for RS-422 signal pairs
35	Spare								
36	Spare								
37	A_IFC_–15_PWR	PWR	16	150	T3-1B		3		–15 V power

Conn. No.		Location	Conn No.	
P732P		<— Cable U15 —>	P631S	P633S
J732S		<— Box-Mounted Receptacles —>	J631P	J633P

IPU							A-BEU	B-BEU	
Pin	**Signal Name**	**Circuit Type**	**V max** V	**I_{max}** mA	**Group**	**Wire Type**	**Pin**	**Pin**	**Function**
38	B_IFC_–15_PWR	PWR	16	150	T3-2B				–15 V power
39	Spare								
40	B_IFC_POWER_SHD				Note 1B			1	Shield for power wire groups
41	B_IFC_SIGNAL_SHD				Note 2B			2	Shield for RS-422 signal pairs
42	IFC_BBFPT2_DRV	AD590						1	BB Front Plate temp. sensor 2
43	IFC_BBFPT2_SEN	AD590							BB Front Plate temp. sensor 2
44	Spare								
Shell	Chassis Ground						Shell	Shell	Overall Cable Shield
	Chassis Ground						9		Chassis pin if required
	Chassis Ground						10	1	Chassis pin if required
	Spare						4		
	Spare						11	1	
	Spare						13	1	
	Spare						18	1	
	Spare						22	2	

Note 1A: this shield to enclose wires to IPU connector pins 6, 7, 21, 22, 37.
Note 1B: this shield to enclose wires to IPU connector pins 8, 10, 24, 25, 38.
Note 2A: this shield to enclose wires to IPU connector pins 1, 2, 3, 4, 5, 16, 17, 18, 19, 20.
Note 2B: this shield to enclose wires to IPU connector pins 11, 12, 13, 14, 15, 26, 27, 28, 29, 30.

3.3 Functional Interface

3.3.1 IPU-to-IFC Control Word Formats

The content of Control Word transfers from the IPU to the BEU shall conform to the formats specified in the following subsections. Bit conventions shall be as follows:

a. Control Words shall be 16 bits in length.

b. Serial binary words shall be transmitted most significant bit (MSB) first.

c. Bits shall be numbered 0 to 15 where the 0 bit is the LSB.

3.3.1.1 Heater Control Word

The Heater Control word shall use the bit assignments shown in Table 3.3.1.1-1:

Table 3.3.1.1-1 IFC Heater Control Word Bit Assignments

IPU CONTROL WORD		
BIT #	CODE	FUNCTION
MSB 15	S	S = 0 for 'A' side; S = 1 for 'B' side; set by IPU
14	I	Ident. bit: always 1 for HCW
13	-	Not used by IFC
12	-	Not used by IFC
11	-	Not used by IFC
10	-	Not used by IFC
9	-	Not used by IFC
8	-	Not used by IFC
7	V7	Value bit #7
6	V6	Value bit #6
5	V5	Value bit #5
4	V4	Value bit #4
3	V3	Value bit #3
2	V2	Value bit #2
1	V1	Value bit #1
LSB 0	V0	Value bit #0

A Heater Control word shall be sent to the IFC once per Major Frame (approximately 1.3 per sec). The value may or may not be the same as the previously-sent value. The timing within the Major Frame is unimportant.

3.3.1.1 Data Request Word

The Data Request word shall use the bit assignments shown in Table 3.3.1.1-1.

One Data Request word shall be sent every Major Frame. The timing within the Major Frame is unimportant, except that interval between the end of one DRW and the beginning of the next shall be not less than 700 ms. Data Request words shall be sent in the sequence DRW0 to DRW7 as shown in Table 3.3.1.1-2.

Table 3.3.1.1-1 IFC Data Request Word Bit Assignments

IPU CONTROL WORD		
BIT #	CODE	FUNCTION
MSB 15	S	S = 0 for 'A' side; S = 1 for 'B' side; set by IPU
14	I	Ident bit: always 0 for DRW
13	DS2	Data Select Bit #2 (MSB)
12	DS1	Data Select Bit #1
11	DS0	Data Select Bit #0 (LSB)
10	-	Not used by IFC
9	-	Not used by IFC
8	-	Not used by IFC
7	-	Not used by IFC
6	-	Not used by IFC
5	-	Not used by IFC
4	-	Not used by IFC
3	-	Not used by IFC
2	-	Not used by IFC
1	-	Not used by IFC
LSB 0	-	Not used by IFC

Table 3.3.1.1-1 IFC Data Request Word Bit Assignments

DATA REQST WORD	<---------- BIT PATTERN ---------->					SELECTED FUNCTION	CORRESPONDING TELEMETRY LIST MNEMONIC *
		DS BITS					
		2	**1**	**0**			
DRW0	S 0	0	0	0	x x x x x x x x x x x	REF. RESISTOR	IFC_REF_TMP
DRW1	S 0	0	0	1	x x x x x x x x x x x	PRT #1	IFCBB_TMP1
DRW2	S 0	0	1	0	x x x x x x x x x x x	PRT #2	IFCBB_TMP2
DRW3	S 0	0	1	1	x x x x x x x x x x x	PRT #3	IFCBB_TMP3
DRW4	S 0	1	0	0	x x x x x x x x x x x	SPARE	
DRW5	S 0	1	0	1	x x x x x x x x x x x	+15V MON	IFC_PSV_P15
DRW6	S 0	1	1	0	x x x x x x x x x x x	-15V MON	IFC_PSV_N15
DRW7	S 0	1	1	1	x x x x x x x x x x x	+5V MON	IFC_PSV_P5

*Note: The telemetry list mnemonic is provided for reference only.

3.3.2 IFC-to-IPU Data Word Formats

The IFC Data Word transfers from the BEU to the IPU shall conform to the following protocol:

a. All IFC Data Words shall be 24 bits in length.

b. Serial binary words shall be transmitted most significant bit (MSB) first.

c. Bits shall be numbered 0 to 23 where the 0 bit is the LSB.

Each IFC Data Word shall be transmitted in response to a Data Request Word. The information content of each IFC Data Word shall correspond to the data specified by the immediately preceding data request word.

3.4 Mechanical Interface

N/A

3.5 Thermal Interface

N/A

3.6 Optical Interface

N/A

3.7 Other Interfaces

N/A

4 ABBREVIATIONS & ACRONYMS

BEU	Black Body Electronics Unit
C&TH	Command & Telemetry Handbook
DRW	Date Request Word
GSFC	Goddard Space Flight Center
HCW	Heater Control Word
IBB	IFC Black Body
ICD	Interface Control Document
IFC	In-Flight Calibrator (Subsystem)
IICD	Internal Interface Control Document
IPS	Instrument Processor Subsystem
IPU	Instrument Processor Unit
ITS	Instrument Technical Specification
LSB	Least Significant Bit
MSB	Most Significant Bit
PPL	Preferred Parts List
TBD	To Be Determined
TBV	To Be Verified

END